LOW-NOISE CIRCUITRY FOR EXTREME ENVIRONMENT DETECTION SYSTEMS IMPLEMENTED IN SIGE BICMOS TECHNOLOGY

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Eleazar Kenyon

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LOW-NOISE CIRCUITRY FOR EXTREME ENVIRONMENT DETECTION SYSTEMS IMPLEMENTED IN SIGE BICMOS TECHNOLOGY

Approved by:

Dr. John D. Cressler, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Gregory D. Durgin
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Ioannis Papapolymerou
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: 2 July 2012

This thesis is dedicated to Sarah, my beloved wife.

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SUMMARY

This work evaluates two SiGe BiCMOS technology platforms as candidates for implementing extreme environment capable circuitry, with an emphasis on applications requiring high sensitivity and low noise.

In Chapter 1, applications requiring extreme environment sensing circuitry are briefly reviewed and the motivation for undertaking this study is outlined. A case is then presented for the use of SiGe BiCMOS technology to meet this need, documenting the benefits of operating SiGe HBTs at cryogenic temperatures. Chapter 1 concludes with a brief description of device radiation effects in bipolar and CMOS devices, and a basic overview of noise in semiconductor devices and electronic components.

Chapter 2 further elaborates on a specific application requiring low-noise circuitry capable of operating at cryogenic temperatures and proposes a number of variants of band-gap reference circuits for use in said system. Detailed simulation and theoretical analysis of the proposed circuits are presented and compared with measurements, validating the techniques used in the proposed designs and emphasizing the need for further understanding of device level low-temperature noise phenomena.

Chapter 3 evaluates the feasibility of using a SiGe BiCMOS process, whose response to ionizing radiation was previously uncharacterized, for use in unshielded electronic systems needed for exploration of deep space planets or moons, specifically targeting Europa mission requirements. Measured total ionizing dose (TID) responses for both CMOS and bipolar SiGe devices are presented and compared to similar technologies. The mechanisms responsible for device degradation are outlined, and an explanation of unexpected results is proposed.

Finally, Chapter 4 summarizes the work presented and understanding provided by this thesis, concluding by outlining future research needed to build upon this study and fully realize SiGe based extreme environment capable precision electronic systems.

CHAPTER I

INTRODUCTION

This chapter addresses the goals and motivation for the presented study and lays the theoretical groundwork for the technical discussion contained in following chapters.

1.1 Motivation

Today the world is in the midst of what some have termed the "Information Age." For over four decades, integrated circuit technologies have followed the exponential growth pattern predicted by Gordon Moore in 1965 [28], driving incredible advances in personal and mobile computing, communications, television and radio broadcasts, and a host of other application spaces. These developments hinge on the ability to rapidly transmit and process digital information in the form of "ones" and "zeros," and to the casual observer it may appear that the world has "gone digital," that digital technology is rapidly superseding the antiquated analog electronics of yesteryear. While there is a kernel of truth to such claims, there is only a kernel; such a statement fails to consider the fact that the physical world we live in is intrinsically analog. While digital processing is largely deterministic, and digital data is represented by discrete voltage levels, the physical universe is fundamentally probabilistic, and physical quantities (on a macroscopic scale) are continuous and typically exhibit random or pseudo-random fluctuations. While digital circuits can perform billions of operations per second on discrete numbers, analog circuits are needed to convert the continuous voltage levels observed in the physical domain into discrete representations intelligible to a digital processor. Thus, digital electronics will forever be dependent on physical transducers to convert physical information into voltage information, and in turn, analog circuitry to sense and discretize continuous voltage levels.

The accuracy of a digital circuit is, to first order, dependent simply on the number of binary digits (or bits) available to represent a given quantity. Physical quantities, however,

even when appearing constant on a macroscopic scale, actually exhibit small, random fluctuations, and are typically described by an average value and a statistical variance. Such random fluctuations, or "noise," as they are called in electronics, limit the ability to precisely measure a given quantity, and unlike digital information, any analog quantity cannot be exactly measured and there will always remain some probabilistic uncertainty as to the actual value of the quantity at a given point in time. Steps can be taken to reduce the uncertainty in such a measurement, and this work will consider the effect of temperature on such uncertainty in electronic detections systems.

Thermal energy typically contributes significantly to noise in an electronic system; thus, one method of reducing uncertainty, or noise, in a measurement system is to operate the circuitry at low temperatures. Some electronics used in applications requiring extreme sensitivity (e.g. particle physics experiments, radio astronomy) may even be operated in cryogenic environments, which results in degraded performance for some devices and circuits optimized for operation at typical earth temperatures. Space-borne electronic detection systems may also face the same difficulties when operating in the ambient environment of an extraterrestrial planet or moon, only the effects of ionizing radiation must also be combatted. Thus, care must be taken when choosing a technology for use in such "extreme environment" applications. Silicon, which is used almost exclusively for digital applications, is the ideal candidate in terms of cost, with extremely mature processing and growth technologies available for the physically abundant material. However, metal oxide semiconductor (MOS) field effect transistors (FETs), the devices used for digital logic circuitry, have undesirable noise characteristics and low radiation tolerances, and silicon based bipolar junction transistors, which show markedly improved noise performance, are unsuitable for use at low temperatures. More exotic III-V semiconductor based bandgap engineered devices with acceptable performance at cryogenic temperatures may be used, but such materials are more expensive and difficult to fabricate and are not suitable for large-scale integrated analog and digital circuits. One technology that has garnered much attention in the past decade as the ideal candidate for extreme environment applications is the silicon-germanium heterojunction bipolar transistor, or SiGe HBT, which uses bandgap engineering to improve

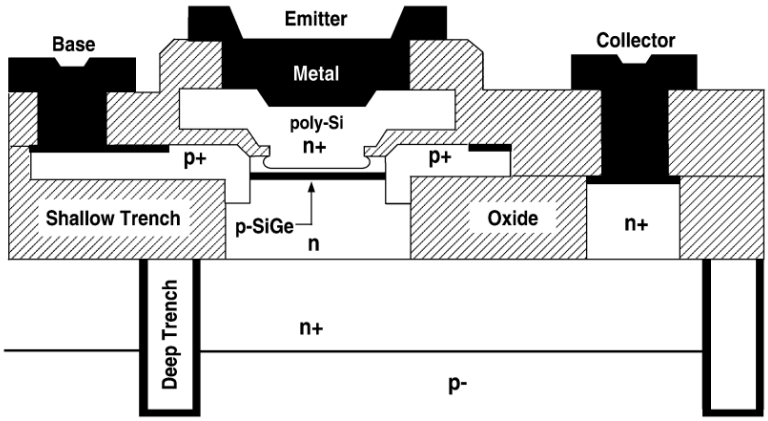

Figure 1.1: Representative cross section of a first generation SiGe HBT (After [10])

speed and temperature characteristics while retaining the cost and integration benefits of silicon [7].

1.2 Silicon-Germanium Technology

The concept of a heterojunction bipolar transistor (HBT) dates back to the invention of the original bipolar transistor by William Shockley in 1951 [31]. Herbert Kroemer then pioneered the theoretical understanding of such a device in 1957 [22], but it was not until three decades later that fabrication technology had progressed sufficiently to enable the first functional silicon based prototype, demonstrated by IBM in 1987 [20]. Today, IBM offers fourth generation SiGe HBTs at a 90nm lithography node that are operable at frequencies over 300GHz, and SiGe BiCMOS is routinely used for high performance analog and mixed-signal, as well as RF applications.

The SiGe HBT achieves its improved performance by modifying the bandgap structure (the bandgap is a range of energies forbidden to carriers in a semiconducting or insulating material) of the base-emitter junction via the insertion of germanium into the HBT's base region. The germanium alloy primarily has one or both of the following effects: an increase in current gain and Early voltage, and a reduction in the time it takes carriers to transit the base region of the device.

The basic operation of a silicon BJT derives from that of a simple p-n junction, in which majority carriers in one region of a semiconductor diffuse into an adjacent region of

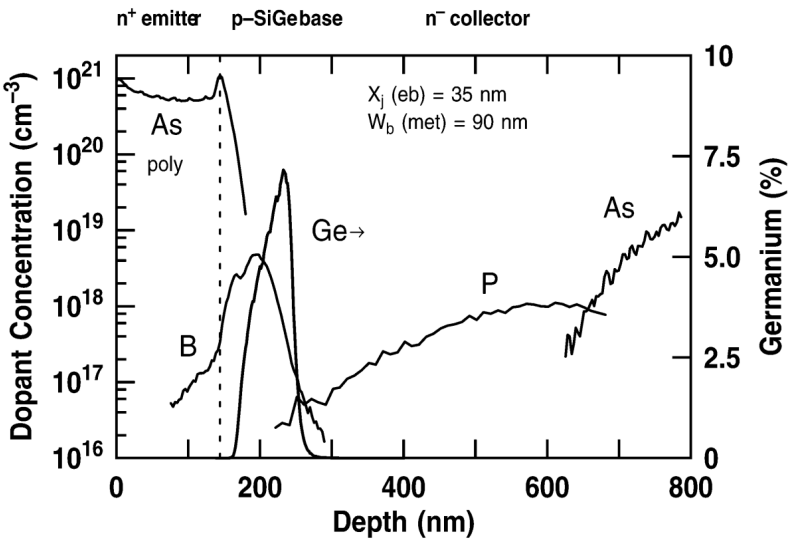

Figure 1.2: Representative doping and germanium profiles of a first generation SiGe HBT (After [10])

opposite doping type, and vice versa. In order to maintain charge neutrality, a "built-in" electric field forms at the junction of the oppositely doped regions, which gives rise to an energy barrier preventing additional carriers from diffusing across the junction. Applying an external voltage across the junction reduces the energy barrier presented by the built-in field, exponentially increasing the number of carriers with sufficient energy to overcome the barrier and diffuse into the adjacent region, producing current flow. If one region is much more highly doped than the other, most of the current will be driven by the majority charge carriers of the more highly doped region; a BJT harnesses this fact to create gain by making the lowly doped region (the base) extremely narrow (much narrower than the diffusion length of a carrier), allowing the charge carriers from the highly doped region (the emitter) to diffuse through the narrow base into a third terminal (the collector) of the same doping type as the emitter. Thus, only a small current (holes diffusing from base to emitter for an NPN device) must be supplied to the base in order to sustain conduction of a much larger current between emitter to collector. In a silicon BJT, the ratio of base current to collector current, or current gain, can be improved by increasing the doping contrast of the highly doped emitter and low doped base, skewing the total junction current toward electron carriers. There are, however, practical limits on doping levels imposed by fabrication and

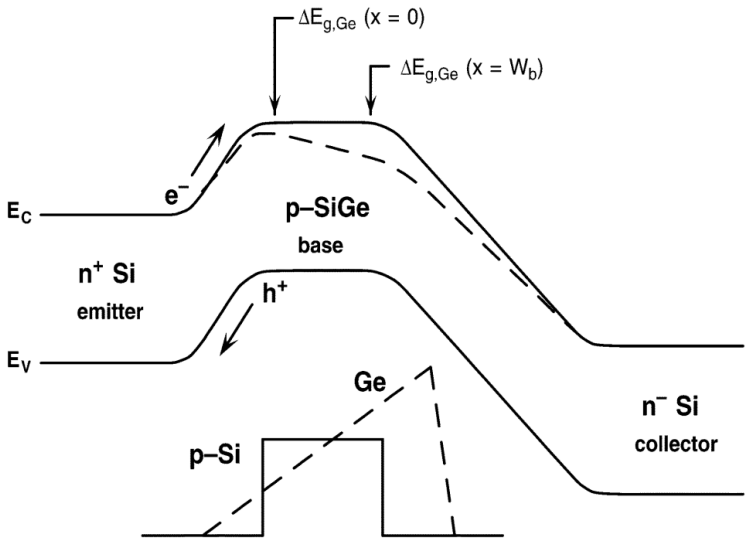

Figure 1.3: Energy band diagram of Si BJT (solid) and SiGe HBT (dashed) operating in the forward active region at low injection (After [10])

performance constraints, as a lower doped base results in a higher intrinsic resistance of the base region, which adversely affects both speed and noise.

The SiGe HBT, on the other hand, improves the ratio of base to emitter current by reducing the energy barrier seen by the electrons in the emitter via bandgap engineering; the presence of germanium in the base lowers the effective bandgap of the material, which reduces the energy level of the conduction band, skewing the junction current towards electrons. This effectively decouples the current gain and base doping, allowing much higher doping concentrations in the base region (and thus lower resistance and noise). While the improvement in current gain depends primarily on the germanium content at the base-emitter junction, a speed improvement can also be achieved by grading the germanium content in the base region, forming a pseudo-electric drift field that "pushes" carriers through the base region, reducing the base region transit time, which is often the dominant factor in the emitter-base diffusion capacitance. Thus, the lower diffusion capacitance of the SiGe HBT enables it to operate at frequencies much higher than those allowed by a standard silicon BJT. To maximize the benefits of these two effects, mutually exclusive germanium profiles must be used, a box for maximal current gain, and a ramp for maximum speed. In practice, a trapezoidal germanium profile is typically used as a compromise between these

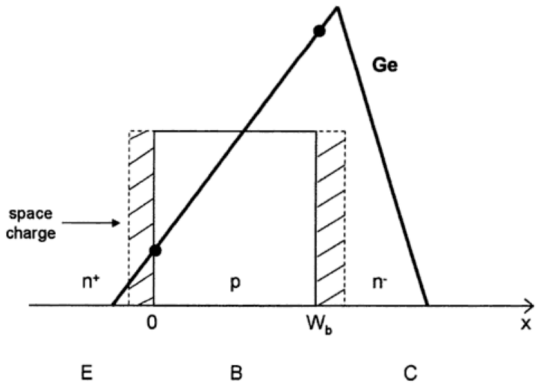

Figure 1.4: Schematic doping and germanium profiles as used in equation derivations (After [10])

two shapes [10]. The extension of the germanium alloy into the collector region also has the effect of improving the Early voltage of the device, which directly impacts the output conductance and intrinsic gain of the HBT.

1.3 Cryogenic Operation of SiGe HBTs

Bandgap engineered devices typically exhibit good temperature characteristics [10], and SiGe HBTs are no exception. Whereas homojunction silicon BJTs experience significant performance degradation at cryogenic temperatures, most relevant circuit parameters of a SiGe HBT (i.e. current gain, transition frequency, and Early voltage) actually improve with decreasing temperature [7]. This is result of the minority carrier operation of bipolar devices since terminal currents are proportional to the square of the intrinsic carrier concentration (n_i^2), which depends exponentially on the bandgap of the material (E_g). Additionally, due to statistical mechanical phenomena, the change in the bandgap parameter will be divided by the thermal energy (kT), establishing an exponential relation between temperature and many device parameters.

The germanium induced improvements in a SiGe HBT with respect to a standard silicon BJT of identical geometry and doping are mathematically described (as derived and presented in [10]) by Eqs. 1.1-1.3. Note that that $\Delta E_{g.Ge}(grade)$ and $\Delta E_{g.Ge}(0)$ are defined as $\Delta E_{g.Ge}(x = W_b) - \Delta E_{g.Ge}(x = 0)$ and $\Delta E_{g.Ge}(x = 0)$, respectively (see Fig. 1.3 and

Fig. 1.4 for graphical representations), where x is a variable used to represent the one-dimensional position with respect to the base-emitter junction, $x = 0$ represents the edge of the intrinsic base at the base-emitter junction, and $x = W_B$ represents the edge of the intrinsic base at the base collector junction. Additionally, $\tilde{\gamma}$ and $\tilde{\eta}$ are unitless numbers less than one which are added to account for density of states and electron diffusivity differences, respectively, in Si and SiGe materials. Finally, it should be noted that the expressions below are derived for a ramp germanium profile. However, the highlighted trends hold for box and trapezoidal profiles as well. Fig. 1.5 shows the predicted performance graphically overlaid with measured results, as presented in [7].

$$\left.\frac{\beta_{SiGe}}{\beta_{Si}}\right|_{V_{BE}} = \frac{\tilde{\gamma}\tilde{\eta}\Delta E_{g.Ge}(grade)/kT e^{\Delta E_{g.Ge}(0)/kT}}{1 - e^{-\Delta E_{g.Ge}(grade)/kT}} \tag{1.1}$$

$$\left.\frac{V_{A.SiGe}}{V_{A.Si}}\right|_{V_{BE}} \simeq e^{\Delta E_{g.Ge}(grade)/kT}\left[\frac{1 - e^{-\Delta E_{g.Ge}(grade)/kT}}{\Delta E_{g.Ge}(grade)/kT}\right] \tag{1.2}$$

$$\frac{\tau_{b.SiGe}}{\tau_{b.Si}} = \frac{2}{\tilde{\eta}}\frac{kT}{\Delta E_{g.Ge}(grade)}\left\{1 - \frac{kT}{\Delta E_{g.Ge}(grade)}\left[1 - e^{-\Delta E_{g.Ge}(grade)/kT}\right]\right\} \tag{1.3}$$

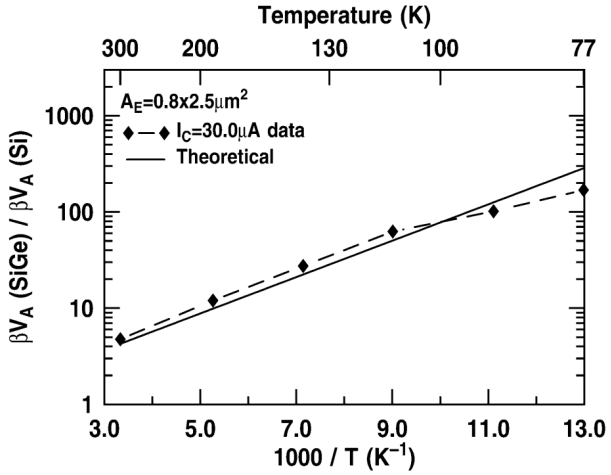

Figure 1.5: Relative improvement of current gain and Early voltage in SiGe HBT over Si BJT across temperature (After [7])

As indicated by Eqs. 1.1-1.3 and supporting figures, Silicon Germanium HBTs demonstrate excellent performance at low and cryogenic temperatures, making them an excellent

candidate for use in cryogenic sensing systems.

1.4 Radiation Effects

Radiation effects are another important consideration in extreme environment electronic operation and must be addressed in the design of space-borne electronic systems [32] or systems used for high energy particle physics experiments (e.g. the Hadron Collider) [13]. High energy particles striking a semiconductor device cause three primary effects: single event effects (SEE), displacement damage (DD), and total ionizing dose (TID) effects.

A single event effect may occur when a highly energetic particle strikes the active area of a biased device and deposits its energy in the material, generating a track of excess electron/hole pairs. Particles with sufficient energy can generate enough carriers to substantially perturb the terminal voltages and currents of the struck device, generating spurious transients in analog circuitry or causing bit errors in digital circuitry.

Displacement damage occurs when energetic particles cause damage to the lattice, potentially generating trap energy levels and/or deactivating dopant atoms, changing the resistivity, and, potentially, other electrical properties of the material.

TID effects are primarly caused by charge trapped in bulk or interface oxides, which generate undesirable electric fields, or by traps created at oxide interfaces, which alter the generation and recombination characteristics of the device in question. This study focuses primarily on this form of radiation damage, and DD and SEE effects will not be discussed further.

In CMOS devices, the two primary TID degradation mechanisms arise from charge trapped in the gate and isolation oxides due to the combination of electric fields in the device and from traps at oxide-semiconductor interfaces. If sufficient charge of the necessary polarity builds up in an oxide surface near the channel, the trapped charge can generate electric fields significant enough to either invert the channel (typically a problem for nFETs) and increase on-state leakage currents, or to alter the threshold voltage (typically increasing in pFETs and decreasing in nFETs with increasing dose). In older technologies with thick gate oxides, TID induced oxide charge often rendered CMOS devices unusable at high doses.

However, smaller lithography processes with highly scaled gate dimensions show little to no gate oxide trapping [30] [12], and isolation oxides are the primary cause of degradation in deep sub-micron CMOS technologies. This scaling trend has enabled some sub-micron CMOS technologies to be operated at very high (multi-Mrad) doses without catastrophic failure [16].

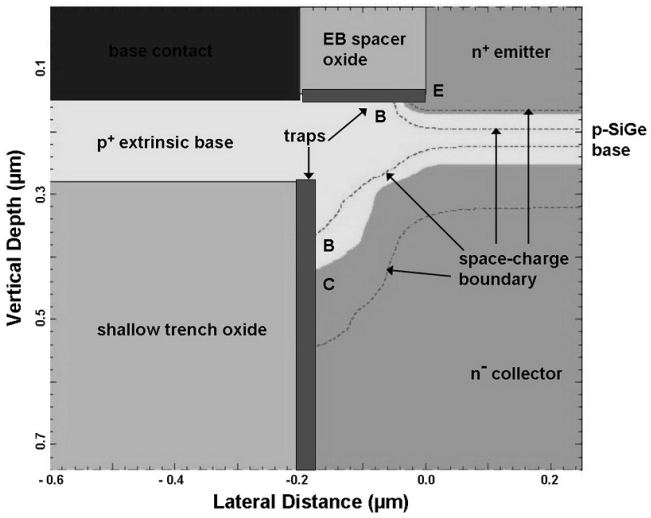

Figure 1.6: Cross section of SiGe HBT illustrating spatial location of radiation induced traps (After [9])

In SiGe HBTs, TID effects are caused primarily by degradation of the emitter-base spacer oxide [9]. Increased trap densities at the oxide interface results in increased generation and recombination of carriers. If carriers are generated in the space charge region, electric fields in the device sweep the carriers through the junction resulting in excess base current with a non-ideal $\frac{2kT}{q}$ slope. This results in degradation of current gain at low current densities. Additionally, studies have shown that radiation also degrades the low-frequency noise performance of SiGe HBTs [2]. Fig. 1.6 schematically shows the spatial location of the radiation induced traps, and Fig. 1.7 shows the response of a typical SiGe HBT forward gummel characteristic with increasing ionizing dose.

1.5 Noise Fundamentals

As stated previously, on a large scale, physical quantities appear to randomly fluctuate about an average value. These fluctuations can result from a large number of sources,

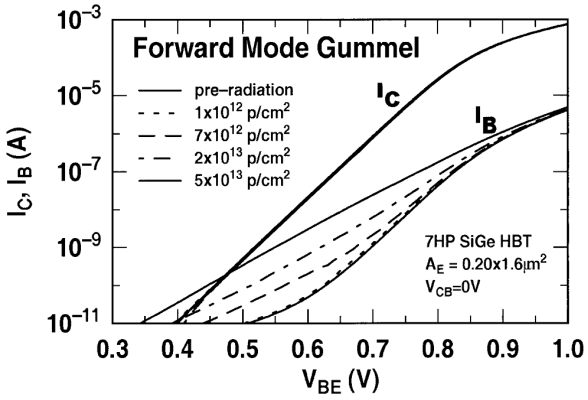

Figure 1.7: Radiation induced degradation of SiGe HBT forward gummel (After [9])

but many such fluctuations deriving from diverse sources share striking similarities. As predicted by the Central Limit Theorem, Normal, or Gaussian distributions are seen in a wide variety of systems. Another type of variance termed flicker or "$1/f$" noise also appears in such diverse systems as the water flow in the Nile river, the luminosity of stars [3], spatial error in human cognition [14], and even the spectral content of music tends to conform to such a pattern [35].

Current and voltage levels in electronic devices are also subject to fluctuation, which, in electronic systems, is called noise. Because this fluctuation, or noise, is a random process and the average value of a given signal does not change, regardless of the magnitude of the fluctuation in a given system, noise is specified as a mean-square value (analogous to the variance of a gaussian or normal statistical distribution). Additionally, noise is specified as density, with respect to frequency, and the integrated noise density in a 1 Hz window at a given frequency is referred to as the "spot noise."

1.5.1 Types of Noise

In semiconductor based electronic systems, there are four primary types of noise: thermal noise, shot noise, $1/f$ noise, and generation/recombination (G/R) or random telegraph signal noise.

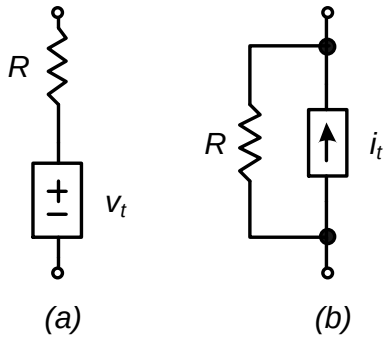

Figure 1.8: Circuit schematic representations of thermal noise in a resistor

1.5.1.1 Thermal Noise

Thermal noise, as its name indicates, is random noise generated by thermally induced carrier motion in resistive materials. Thermal noise exists in any resistive material, and its mean square value is directly proportional to absolute temperature. In a circuit context, thermal noise can be represented as either a voltage source in series with the resistance, or a current source in parallel with the resistance (shown schematically in Fig. 1.8). Thermal noise is "white noise," or noise that does not show any frequency dependence and has equal amplitude at all frequencies.

Eqs. 1.4 and 1.5 give the mathematical expressions for the mean-square amplitude of the noise sources (depending on the chosen model) in a resistor of value R. Note that k is Boltzmann's constant, and T is absolute temperature.

$$\overline{i_t{}^2} = \frac{4kT\Delta f}{R} \tag{1.4}$$

$$\overline{v_t{}^2} = 4kT\Delta f R \tag{1.5}$$

Additionally, it can be shown that any purely resistive network can be reduced to an equivalent resistance and that the the noise in such a network can be accurately modeled as the noise of a simple resistance whose value is equivalent to that of the resistive network [23].

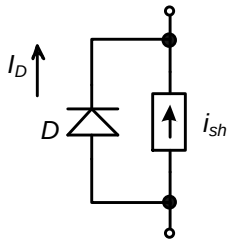

Figure 1.9: Circuit schematic representation of shot noise in a diode

1.5.1.2 Shot Noise

Shot noise exists in any semiconductor device where DC current flows through a potential barrier (e.g. a *pn* junction). As discussed previously, a *pn* junction conducts current when carriers have enough energy to overcome the potential barrier imposed by the junction's built-in electric field. Thus, the current in such a device is composed of many individual "pulses" as each unit charge (i.e. the charge of an electron or hole) passes over the barrier. The total number of carriers at a given moment possessing sufficient energy to pass over the barrier and diffuse away on the other side of the junction varies with time, giving rise to changes in the instantaneous current. This variation results in shot noise, whose mean-square noise current varies directly with DC current (see Eq. 1.6). This type of noise depends only on DC current, is independent of temperature, and like thermal noise, has a white spectrum with no frequency dependence. In reality, shot noise begins to drop off at sufficiently high frequencies due to device parasitics, but for the purposes of this study it will be considered to be purely white noise.

$$\overline{{i_{sh}}^2} = 2qI_D\Delta f \tag{1.6}$$

Schematically, shot noise can be modeled with a current source in parallel with the diode or junction in question (See Fig. 1.9).

1.5.1.3 $1/f$ Noise

The mean-square noise density of $1/f$ noise, as its name indicates, decreases with increasing frequency. This type of noise is seen nearly universally in a broad range of systems, and there have been attempts to probe the underlying mechanisms of $1/f$ noise and uncover unifying principles of such noise [3][21]. However, to the author's knowledge, no consensus has been reached on a comprehensive unified theory of $1/f$ noise.

In semiconductor materials and devices, it is has been shown and generally accepted that $1/f$ noise is caused by fluctuations in the bulk conductivity of the semiconductor [17]. However, there remains considerable debate as to the source of the conductivity changes, with some suggesting that the phenomenon occurs due to carrier number fluctuations and others claiming a mobility fluctuation mechanism. While $1/f$ noise is typically only observed when direct current flow is present, the conductivity fluctuation exists independently of current, and the current is simply needed to convert the conductivity fluctuation into voltage and current noise [17]. Regardless, $1/f$ noise is modeled as a current source whose mean square value is given in Eq. 1.7 [15], where K_f is a constant that varies with device and, potentially, temperature, I is the DC current in the component in question, a is an exponent typically varying between 0.5 and 2, and b is a constant of roughly unity. In the case that the frequency exponent, b, is exactly equal to one, such a noise spectrum is called "pink noise," and has equal power per octave or decade for all frequencies.

$$\overline{{i_f}^2} = \frac{K_f I^a \Delta f}{f^b} \tag{1.7}$$

$1/f$ noise is present in a practically any electronic component with a direct current flow, including resistors and any type of transistor, regardless of structure or material. Another important trend is the scaling of the KF parameter with area. In general, $1/f$ noise in transistors and resistors increases with scaling, and for a fixed current, KF is inversely proportional to the device area, $W \times L$ for CMOS transistors and resistors, and $W_E \times L_E$ for bipolar transistors.

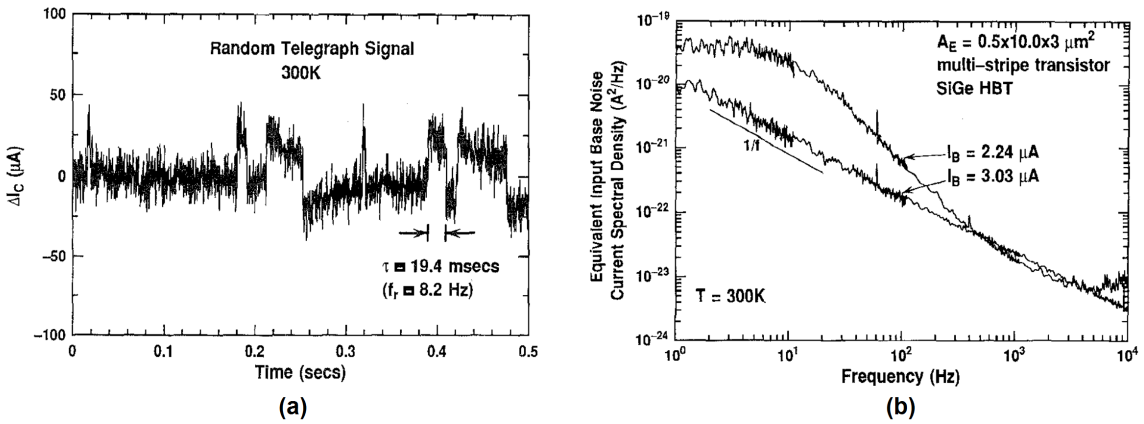

Figure 1.10: RTS noise in a SiGe HBT in both time (a) and frequency (b) domains (After [34])

1.5.1.4 Random Telegraph Signal Noise

Random telegraph signal (RTS) noise (sometimes called "burst" or "popcorn" noise) is another frequency dependent noise mechanism. When viewed on an oscilloscope, this type of noise shows sharp transitions between two or more discrete current values. RTS noise is caused by trapping and release of carriers in the bulk silicon, with transitions between discrete current levels caused by trapping of individual carriers. In the frequency domain, RTS noise remains constant at low frequencies and at some corner frequency (f_c), begins to roll of with a $\frac{1}{f^2}$ slope. Eq. 1.8 describes the general form of RTS noise mathematically [15], and Fig. 1.10 shows its effects graphically. Note that K_{RTS} is a constant value dependent on device and temperature, c is an exponent between 0.5 and 2, and f_c is the corner frequency of the RTS noise spectrum.

$$\overline{{i_{RTS}}^2} = K_{RTS}\frac{I^c}{1+(\frac{f}{f_c})^2}\Delta f \tag{1.8}$$

1.5.2 Device Noise Models

In semiconductor devices, one or more of the previously described noise phenomena may be present. To aid in understanding the noise characteristics of a circuit containing multiple devices, the small signal models of relevant devices will be shown, including noise sources.

1.5.2.1 Bipolar Junction Transistors

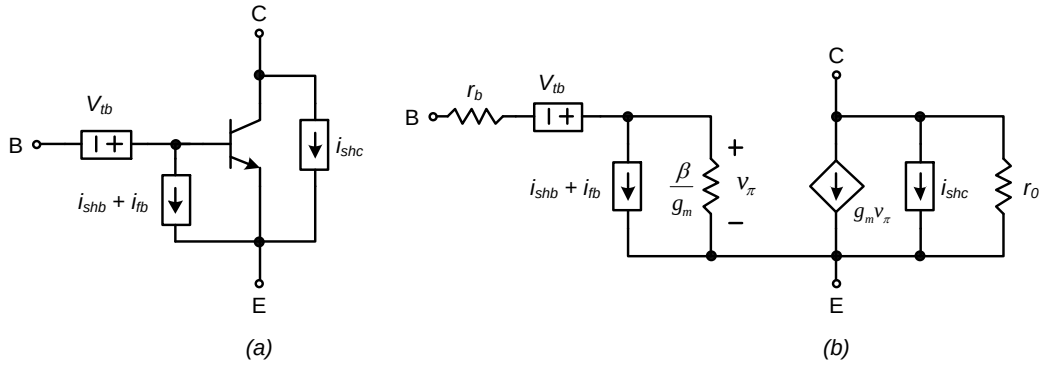

Figure 1.11: Noise sources in a small signal bipolar junction transistor model

Bipolar transistors may show all four of the previously describe noise types. All parasitic resistances generate thermal noise, but the parasitic resistance in series with the base terminal is typically the most significant for device operation. Additionally, the forward biased base-emitter junction results in a shot noise component in both the base and collector currents. The base current of a bipolar transistor also shows $1/f$ noise characteristics (due to surface states at the EB spacer oxide) and potentially RTS noise, although RTS noise is less predictable than other types. Fig. 1.11 shows the small signal model of a bipolar transistor with significant noise sources included.

The broadband and low-frequency noise characteristics of a SiGe HBT do not appreciably differ from an identically constructed Si BJT [10], although the germanium does provide indirect benefits. The increase in the current gain of the SiGe HBT enables the HBT to achieve performance (which, to first order, depends on collector current) equivalent to that of a Si BJT for less base current. This results in improved low-frequency noise performance for the SiGe HBT because the flicker noise is proportional to the base current in the device. Additionally, the germanium allows much higher base doping, which reduces the intrinsic base resistance, r_b, and thermal noise, v_{tb}.

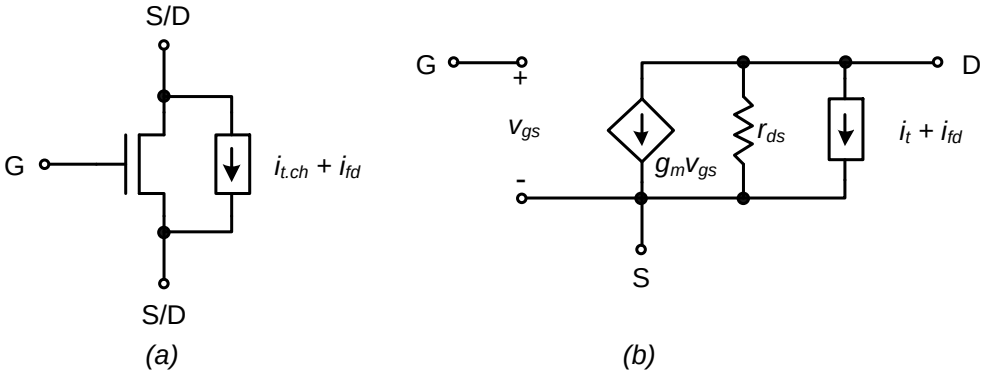

Figure 1.12: Noise sources in a MOS transistor schematic and small signal model

1.5.2.2 CMOS Transistors

CMOS transistors (both n and p-type) show predominantly flicker and thermal noise. The thermal noise is caused by the resistive channel of the device, and the equivalent resistance of the channel is approximately equal to $\frac{2}{3}g_m$, where g_m is the transconductance of the device. The thermal noise of the channel is modeled as a current source connecting from source to drain. The flicker noise component in CMOS transistors can be quite high [15] since the current carriers in the CMOS device are conducted in a thin channel adjacent to the oxide-semiconductor interface. This interface can have a high density of surface states, which results in the trapping and release of carriers, creating a characteristic $1/f$ noise component. Any gate to channel leakage current will also exhibit shot noise; however, because the gate current in a properly functioning device is orders of magnitude less than the channel current, the noise contribution of the gate current can typically be safely neglected and will be in the following chapters. Figs. 1.12a & 1.12b show the schematic drawing and small signal model, respectively, of a CMOS transistor including significant noise sources.

In CMOS and bipolar transistors, the corner frequency is a common figure of merit for low-frequency noise performance. The corner frequency is defined as the point where the magnitude of the input referred $1/f$ noise component is equal to the magnitude of the input referred white noise component of a given transistor. In CMOS transistors, this frequency may extend into the MHz regime, and as a rule of thumb, the corner frequency frequency

of bipolar transistors is one or two orders of magnitude lower than that of their CMOS counterparts.

1.5.2.3 Resistors

As stated previously, resistors generate thermal noise which can be represented as either a current or voltage source (see Fig. 1.8). However, most resistors also have a non-negligible $1/f$ noise component, typically called "excess noise" in the case of a resistor. This excess noise can be modeled as an additional current source in parallel with the resistor, similarly to the thermal noise source of Fig. 1.8b. The flicker noise coefficient KF, and therefore corner frequency, of the resistor varies depending on the resistor type and fabrication.

1.6 Summary

In this chapter, the basic operation of the SiGe HBT and its utility in extreme environment applications has been described. Additionally, the effects of cryogenic operation and ionizing radiation of SiGe HBTs has been discussed, as well as TID effects in MOSFETs. A brief description of fundamental noise phenomena has also been included and supplemented with device level noise models. These factors illustrate the utility of SiGe BiCMOS technology for use in low-noise sensing systems operating in extreme temperature and radiation environments. While many device level studies have been performed previously, this study couples a device level understanding of noise in analog circuits with the design of simple circuits illustrating the advantages, tradeoffs, and limitations of SiGe BiCMOS technology for low-noise analog applications and highlights the need for further understanding of temperature effects in low-frequency noise.

CHAPTER II

LOW-NOISE BAND-GAP REFERENCE DESIGN

This chapter will discuss the motivation for and implementation of a number of variants of band-gap reference circuits, with particular emphasis on constraints imposed by cryogenic operation and noise considerations. The measurement environment is also described and discussed, and measured noise data is presented and compared to the expected theoretical and simulated values.

2.1 Introduction

The design of a band-gap voltage reference (BGR) was initially conceived of by Robert Widlar and published in 1970 [36]; the circuit used only components integrated on a single chip to generate a temperature independent voltage. Since its inception, the band-gap cell has become ubiquitous in integrated circuit applications and forms the basis of almost any integrated voltage reference circuit. In this study, a simplified form of Widlar's initial circuit has been designed and implemented along with another simple variant, the comparisons of which highlight the tradeoffs and constraints associated with each design.

2.1.1 Motivation

To the casual observer, the generation of a stable voltage point may seem a trivial matter, but in practicality, it is a fundamentally challenging problem impacting the performance of many analog circuits and systems. For example, an analog-to-digital converter (ADC) requires a stable analog voltage with which to compare the incoming signal to be digitized, and the achievable resolution of the system depends not only on the noise of the comparison circuitry, but also on the accuracy of the voltage the signal is compared against. Additionally, voltage regulators, which ideally generate a stable, quiet rail voltage from a noisy or inaccurate supply must necessarily be capable of generating accurate voltage levels independent of its input voltage. Both of these applications demonstrate the need for an

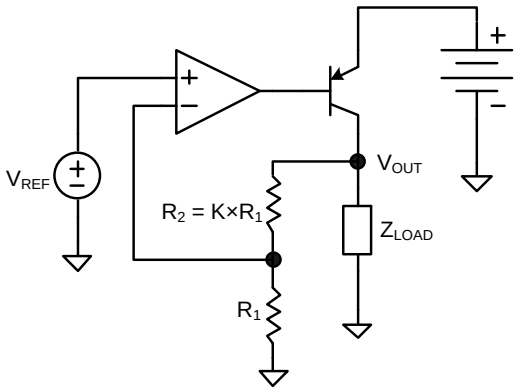

Figure 2.1: A typical circuit implementation of a voltage regulator

accurate, internally generated voltage. External voltages are typically too inaccurate for precision applications. For instance, DC voltage supplies generated from rectifiers or DC-DC converters have vestigial AC content that couples into the powered system as noise, and a battery's voltage can change dramatically over its lifetime and during a single discharge cycle. These constraints require that the generated voltage be referenced to fundamentally unchanging quantities or signals.

The system targeted by the following designs is a cryogenically operated voltage regulator, whose simplified architecture is shown in Fig. 2.1. The proposed regulator would generate the voltage rail needed for low noise detection circuitry used in particle physics experiments and would be required to operate at liquid Argon temperatures. The circuit operates using a feedback loop to set the output voltage V_{OUT} equal to an amplified version of the reference voltage ($K \times V_{REF}$). Thus, the accuracy of V_{OUT} is not only affected by the dynamic characteristics and offset of the amplifier, but any variation in V_{REF} will also appear at the output amplified by a factor of K. Therefore, the output noise of the voltage reference should be made smaller than or comparable to the input referred noise of the amplifier in order to minimize the total noise at the output of the regulator.

Operation at cryogenic temperatures is helpful in reducing the levels of thermal noise in devices and circuits, but it also adds additional constraints. For instance, the turn-on voltages of CMOS and bipolar devices increases at low temperatures, and care must be taken

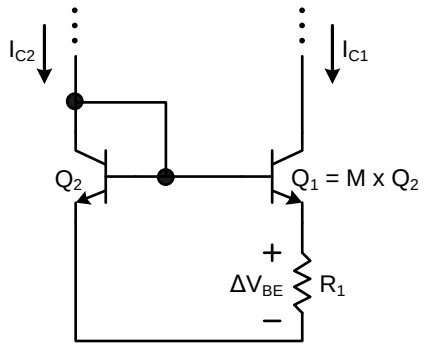

Figure 2.2: A ΔV_{BE} generator circuit

to ensure adequate headroom at operating temperatures. Additionally, commercial devices and circuits are not rated or modeled for the extreme temperatures in question, making it impossible to effectively simulate circuit behavior and necessitating a deep theoretical understanding of the circuits in question. Finally, the circuit should be designed such that performance is not dependent on parameters that may vary widely with process or temperature (e.g. current gain).

2.1.2 Basic Operation of Band-gap References

In the most fundamental sense, a band-gap reference simply adds a thermal voltage, which increases proportionally to absolute temperature (PTAT), to the on-voltage of a diode or bipolar transistor's base-emitter junction, which varies complementary to absolute temperature (CTAT). The summation of the PTAT and CTAT voltages can be scaled such that there is, to first order, no temperature induced variation. A thermal voltage is typically generated using a mismatched bipolar current mirror or a mismatched differential pair input stage. In this design, a mismatched current mirror was used, as shown in Fig. 2.2.

If an identical collector current is forced in both transistors (i.e. using a current mirror), the resulting voltage across the resistor is the difference between the base emitter voltages of Q_1 and Q_2. This difference in V_{BE} is created by the mismatch in the current densities of two transistors, and can be analytically derived by generating an equality using the ideal diode equation (Eq. 2.1) and assuming that the collector currents are equal (see Eq. 2.2). Solving

the equality gives the resulting equation for the collector current in the ΔV_{BE} generator circuit (see Eq. 2.3).

$$I_C = I_S \times e^{\frac{V_{BE}}{V_T}} \tag{2.1}$$

$$\underbrace{V_T \ln \frac{I_C}{I_S}}_{V_{BE1}} = \underbrace{V_T \ln \frac{I_C}{MI_S}}_{V_{BE2}} + \underbrace{I_C R}_{\Delta V_{BE}} \tag{2.2}$$

$$I_C = \frac{V_T \ln M}{R} \tag{2.3}$$

The V_{BE} of a BJT is described in Eq. 2.4 [36], where T_0 is the temperature of interest, V_{BE0} is the V_{BE} at the temperature of interest, and V_{g0} is the band-gap of silicon extrapolated to 0 kelvin. The temperature-stable reference voltage is generated by adding an amplified thermal voltage to a V_{BE} (Eq. 2.5); the value of V_{REF} at which there is no temperature drift can be found by setting the partial derivative of V_{REF} with respect temperature equal to zero (Eq. 2.6, after [36]), which indicates that the temperature induced drift is minimized when V_{REF} is equal to V_{G0}. For bulk silicon, V_{G0} is typically between 1.20V and 1.25V, however, for the designs in question, the optimal reference value was consistently closer to 1.12V, which is likely a result of the reduced bandgap of the SiGe epitaxial base at the base-emitter junction.

$$V_{BE} \cong V_{g0}(1 - \frac{T}{T_0}) + V_{BE0}(\frac{T}{T_0}) \tag{2.4}$$

$$V_{REF} = V_{BE} + KV_T \tag{2.5}$$

$$\frac{\partial V_{REF}}{\partial T} = \frac{V_{BE0}}{T_0} - \frac{V_{G0}}{T_0} - K\frac{V_T}{T_0} \tag{2.6}$$

It should be noted that this description of temperature compensation is abbreviated and only considers the effects of first order (linear) temperature dependencies. If the operating temperature (and hence V_{REF}) varies from its optimal value, second and third order nonlinearities begin to affect the temperature dependence of V_{REF}. While much work has been done and many techniques have been developed for compensating these second and

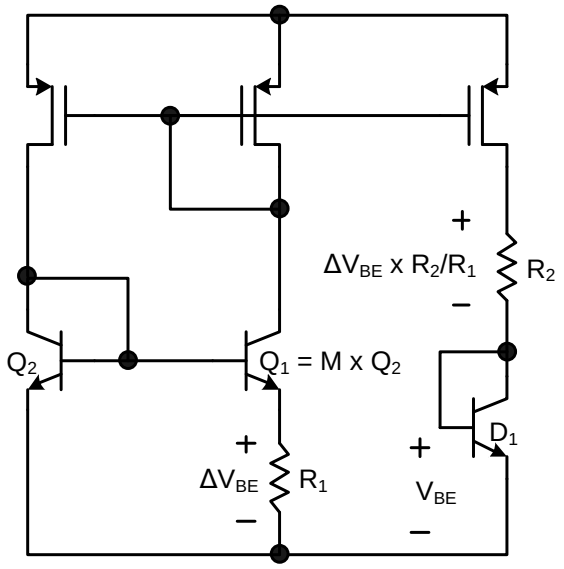

Figure 2.3: A simple band-gap reference implemented using PTAT current source

third order terms, achieving sub 10ppm/°C stability, for the purposes of this study, simple first order compensation is sufficient, and higher order compensation techniques will not be discussed.

2.2 Proposed Circuit Topologies

In order to meet the requirements of the target application, the voltage reference circuits were designed to operate at a supply voltage of 2.1 volts. This constraint, coupled with the fact that transistor turn-on voltages increase at cryogenic temperatures, precluded the use of topologies cascading more than two transistors. Additionally, due to the lack of modeling at cryogenic temperature as well as the noise requirements, a minimalist circuit solution that can be well understood analytically is desired. Fig. 2.3 shows a simple implementation of a band-gap reference using the previously described ΔV_{BE} Generator and a current mirror load. One drawback of using this circuit is the effect of finite current gain on the accuracy of the current generated, because the validity of the result derived in Eq. 2.3 depends on the collector currents of Q_1 and Q_2 being accurately matched. The base currents of both NPN transistors are subtracted from the collector current of Q_2, reducing accuracy.

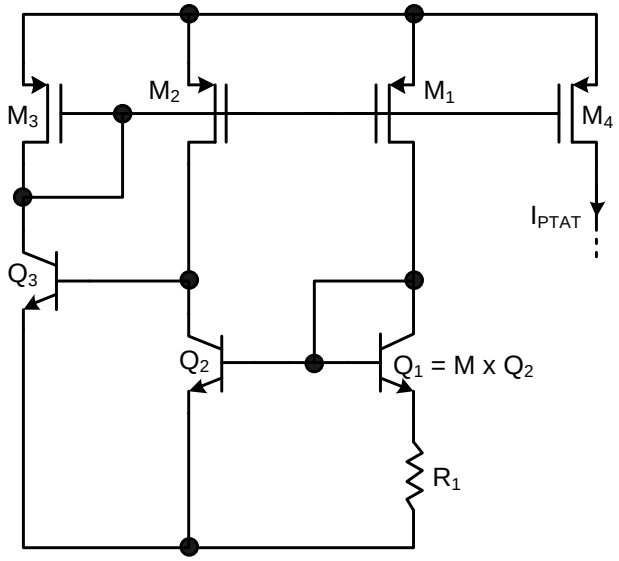

Figure 2.4: An improved PTAT current source

Additionally, V_{DS} mismatch in the current mirror load also contributes to mismatch in the collector currents of Q_1 and Q_2. Finally, the supply rejection of the circuit is related to the intrinsic gain of a single pFET ($g_m \times r_{sd}$), which is generally on the order of 100. For better supply rejection, either a cascode must be used (which is prohibited due to headroom constraints) or additional gain must generated and applied via feedback.

2.2.1 PTAT Current Reference

In order to improve supply rejection and to mitigate the effects of the base current, an improved version of this circuit employing an additional branch, adapted from [19], was used (circuit shown in Fig. 2.4). This topology reduces systematic errors caused by V_{DS} differences in the mirror load (or, conversely, V_{CE} differences in Q_1 and Q_2), and because M_3 is scaled to be twice the size of M_2 and M_1, the base current of Q_3 duplicates the effect of the bases of Q_1 and Q_2, better matching the collector currents of Q_1 and Q_2. Finally, the addition of the Q_3 branch increases the supply rejection of the current source by improving the open loop gain of the feedback amplifier. This can be understood by considering the supply voltage to be the input of a voltage mixing feedback amplifier. Whatever current

is injected into the mismatched NPN mirror is amplified and fed back to the gate of the mirror devices; this amplification factor is increased by the current gain of Q_3 in the circuit of Fig. 2.4. Thus, the current generated by the improved circuit of Fig. 2.4 will be much closer to the ideal value derived in Eq. 2.3 than the current in the circuit of Fig. 2.3 due to improvements in both matching and supply sensitivity.

2.2.1.1 Noise Analysis

Due of the lack of valid simulation models at the temperatures of interest, a detailed understanding of the noise of the circuit is desirable. By using a combination of node and loop equations as well as two port feedback models, a test current source was driven into each node, and the gain at the output of the current reference was analytically calculated and compared to simulation at room temperature to ensure accuracy. The analytical values could then be extrapolated to cryogenic temperatures. Note that for the following derivations, the output conductance of all transistors is assumed to be infinite, which, as verified via simulation, does not appreciably affect the validity of the result. Additionally, all parasitic device resistances and their noise are ignored.

Fig. 2.5 illustrates the technique used to calculate the noise of the circuit. The small-signal gain of a test current source at each node is calculated with respect to i_{out}, which can then be applied to the individual noise sources of each device. To begin, it will be assumed that $\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{1}{2}\frac{W_3}{L_3}$. It will also be assumed that $\frac{W_4}{L_4} = n\frac{W_{1,2}}{L_{1,2}}$ and that all current mirrors operate ideally (i.e. the effects of V_{DS} and V_{CE} mismatch are ignored). Finally, the transconductances of the NPNs will be represented as g_{mnx}, and the transconductances of the pFETs will be represented as g_{mpx}, where x is a numeric value used to identify each device contained in the circuit.

Beginning with the test current source i_{t1}, one can save a great deal of algebra by realizing that the small-signal current flowing into the base of Q_3 is equal to the difference of i_{d2} and i_{c2} and that i_{c2} can be directly related to i_{d2} due to the mirror equality. It can be shown that any current flowing into Node 1 will be amplified at the collector of Q_2 (assuming $g_{mn1} = g_{mn2} = g_{mn}$) by a factor of $1 + g_{mn}R_1$, or $1 + \ln M$. Recall that the

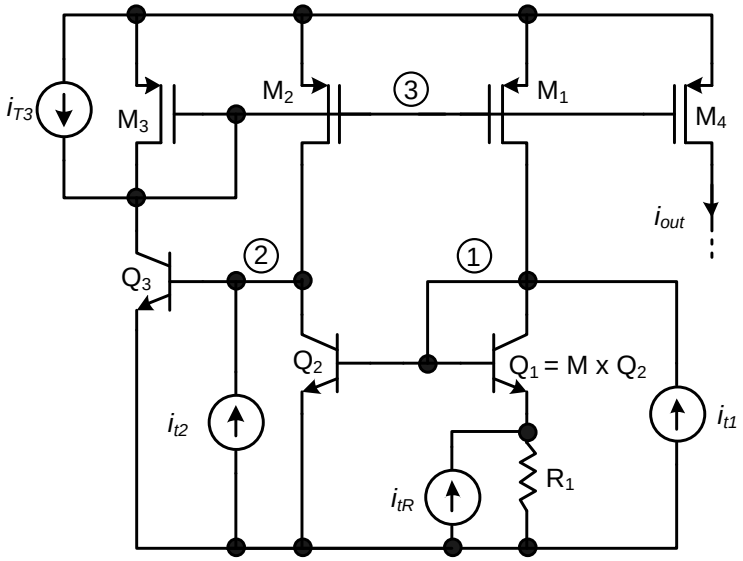

Figure 2.5: Test current sources illustrating calculation of gain from each node to output.

collector current of Q_1 and Q_2 is set by the value of R_1 and M, the emitter scaling factor, from which the $\ln M$ term results. Thus, because both i_{d1} and i_{d2} can be related to the output current, a single node equation can be written for Node 2, which can then be solved, as shown in Eq. 2.7.

$$i_{t1}(1+\ln M) + \underbrace{\frac{i_{out}}{n}}_{i_{d1}}(1+\ln M) - \underbrace{\frac{i_{out}}{n}}_{i_{d2}} = \underbrace{\frac{2i_{out}}{n}}_{i_{d3}}\frac{1}{\beta_3} \quad \Rightarrow \quad \frac{i_{out}}{i_{t1}} = \underbrace{\frac{-n(1+\ln M)}{\frac{2}{\beta_3}+\ln M}}_{A_{i1}} \tag{2.7}$$

The gain of the test current source i_{t2} can be solved using a current feedback amplifier model, where the open loop gain (shown in Eq. 2.8 can be found by "zeroing" the transconductors of Q_2 and M_2. The feedback factor is given in Eq. 2.9, and the closed loop solution is shown in Eq. 2.10.

$$A_{i2.OL} = \frac{i_{out}}{i_{b2}} = \frac{\beta_3 n}{2} \tag{2.8}$$

$$\beta_{fb.i2} = \frac{-i_{d2} - i_{c2}}{i_{out}} = \frac{\ln M}{n} \tag{2.9}$$

$$A_{i2} = \frac{A_{i2.OL}}{1 + A_{i2.OL}\beta_{fb.i2}} = \frac{\beta_3 n}{2 + \beta_3 \ln M} \cong \frac{n}{\ln M} \tag{2.10}$$

Again, note that test current sources were injected in simulation identically to the circuit used for the previous theoretical calculation, and at room temperature the calculated value was within 5% of the simulated value.

Solving for the gain of test current source i_{t3} can also be accomplishing using a current feedback amplifier model. The steps used to solve for i_{t2} are repeated in Eqs. 2.11, 2.12, and 2.13, where the open loop gain is found by "zeroing" the transconductor of Q_3.

$$A_{i3.OL} = \frac{i_{out}}{-i_{d3}} = \frac{-n}{2} \tag{2.11}$$

$$\beta_{fb.i3} = \frac{i_{c3}}{i_{out}} = -\frac{\beta_3 \ln M}{n} \tag{2.12}$$

$$A_{i3} = \frac{A_{i3.OL}}{1 + A_{i3.OL}\beta_{fb.i3}} = -\frac{n}{2 + \beta_3 \ln M} \tag{2.13}$$

Finally, the gain of the test source in parallel with R_1 can be found trivially by relating it to Node 1 via a Norton equivalency, which can then be multiplied by A_{i1}, resulting in Eq. 2.14.

$$A_{iR} = \frac{\ln M}{1 + \ln M} A_{i1} \tag{2.14}$$

Given the previously derived relations, it is possible to translate the significant physical noise sources to the output of the circuit. Note that the noise contributed by parasitic resistances, including base resistance, has been neglected in the following calculations. The expression for the total mean square output noise current of the improved PTAT current source is shown in Eq. 2.15, where $\overline{i_{tmX}{}^2}$ and $\overline{i_{fdX}{}^2}$ are the mean square thermal and flicker noise currents, respectively, of pFET M_X, $\overline{i_{shcX}{}^2}$, $\overline{i_{shbX}{}^2}$, and $\overline{i_{fbX}{}^2}$, are the mean square collector shot noise, base shot noise, and base flicker noise, respectively, of NPN Q_X, and $\overline{i_{trX}{}^2}$ and $\overline{i_{frX}{}^2}$ are the thermal and excess noise of resistor R_X.

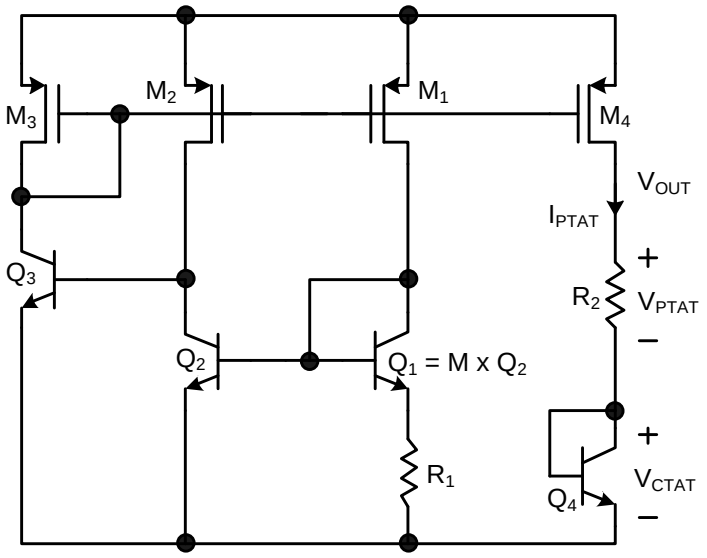

Figure 2.6: Simple BGR using PTAT current source and diode.

$$\begin{aligned}\overline{i_{n.iptat}{}^2} = \quad & \left(\overline{i_{tm1}{}^2} + \overline{i_{fb1}{}^2} + \overline{i_{fb2}{}^2}\right) A_{i1}{}^2 + \\ & \left(\overline{i_{tm2}{}^2} + \overline{i_{shc2}{}^2} + \overline{i_{fd2}{}^2} + \overline{i_{fb3}{}^2}\right) A_{i2}{}^2 + \\ & \left(\overline{i_{tm3}{}^2} + \overline{i_{shc3}{}^2} + \overline{i_{fd3}{}^2}\right) A_{i3}{}^2 + \\ & \left(\overline{i_{tr1}{}^2} + \overline{i_{fr1}{}^2}\right) A_{iR}{}^2 + \\ & \left(\overline{i_{shc1}{}^2} + \overline{i_{fb1}{}^2}\right) (A_{i1} - A_{iR})^2 \end{aligned} \tag{2.15}$$

It should also be noted that base shot noise currents of the NPNs are neglected because their magnitudes are by definition β times smaller than a collector shot noise source, and can be safely neglected.

2.2.2 Simple BGR Design

The PTAT current source can be used to generate a very simple variant of BGR by converting the PTAT current to voltage using a resistor and summing that voltage with a CTAT diode voltage. The resulting circuit is shown in Fig. 2.6.

The noise performance of this circuit is directly limited by the noise of the PTAT current

reference, because any current noise is converted directly to voltage noise via the load resistance, R_2, and small signal diode impedance, $1/g_{mn4}$. Additionally, R_2 must be large enough to amplify the PTAT ΔV_{BE} enough to counter the CTAT diode voltage, constraining the load resistance. The output noise of this simple BGR is given in Eq. 2.16, assuming that $r_{sd4} \gg R_2 + \frac{1}{g_{mn4}}$.

$$\begin{aligned} \overline{v_{n.bgr}{}^2} &= \overline{i_{n.iptat}{}^2}\left(R_2 + \frac{1}{g_{mn4}}\right)^2 + \left(\overline{i_{t2}{}^2} + \overline{i_{fr2}{}^2}\right) R_2 + \frac{\overline{i_{shc4}{}^2} + \overline{i_{fb4}{}^2}}{g_{mn4}{}^2} \\ &\approx \overline{i_{n.iptat}{}^2}\left(R_2 + \frac{1}{g_{mn4}}\right)^2 \end{aligned} \tag{2.16}$$

It can be seen from Eq. 2.16 that the noise of the reference devices is necessarily amplified at the output of the BGR. In the case of this design, the ΔV_{BE} must be amplified by a factor of eight in order to achieve temperature invariance. Thus, the multiplication of the mirror factor n and the ratio $\frac{R_2}{R_1}$ must be equal to eight, which limits design flexibility. As mentioned previously, CMOS devices typically have much higher levels of $1/f$ noise than their bipolar counterparts, and therefore at low frequencies, the flicker noise of the pMOS transistors dominates the simulated output noise of the circuit. One potential solution to this problem is the use of PNP devices in place of pFETs. Lateral PNPs typically have very low current gain compared to a SiGe HBT, and at cryogenic temperatures are practically unusable. The IBM process used in this study, however, has vertical silicon PNP devices, which have substantially higher current gain than a lateral PNP. While the current gain at low temperatures does decrease, the design of the PTAT reference is such that the error caused by the finite base impedance of the PNPs is minimized by the feedback loop.

Fig. 2.7 shows a second variant of the simple BGR circuit employing a PNP rather than pMOS based current mirror. The PNP bipolar transistors have much lower flicker noise coefficients, which in simulation greatly reduces the corner frequency of the BGR output noise spectrum. The two variants were optimized slightly differently, but both the pMOS and the PNP based circuits consumed roughly $5\mu A$ of current per branch in room temperature simulations. Additionally, degeneration resistors were added at the sources of pFET mirror devices to reduce the $1/f$ noise levels as well as at the emitters of the PNP

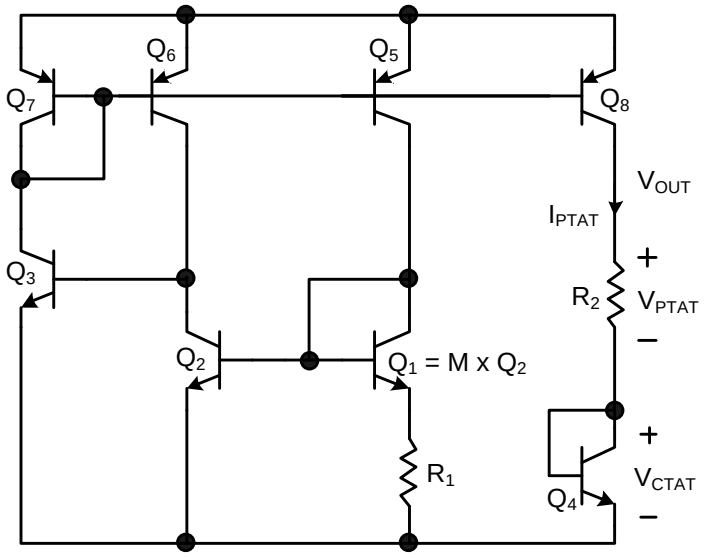

Figure 2.7: Simple BGR substituting vertical PNP BJTs in place of pFETs.

mirror to reduce the white noise levels. One variant using a PNP mirror without emitter degeneration was also fabricated. In order to determine the expected noise of the PNP circuit, the expression for shot noise can be substituted for the channel thermal noise of the pFETs.

By substituting the final component design values into the previously derived analytical noise expressions, the expected white noise level of the BGR using pFETs at room temperature was determined to be 186 $nV/\sqrt{Hz}$, while the simulated value was 191 $nV/\sqrt{Hz}$. The values implemented in the final design were $M = 8$, $n = \frac{(W/L)_4}{(W/L)_{1,2}} = 4$, and $(W/L)_3 = 2 \times (W/L)_{1,2}$. For the PNPs, the emitter areas were scaled by the same amounts such that the mirror behaved identically to the pFET version.

Note that for the pFET variant, the degeneration resistors did not appreciably affect the white noise at the output of the circuit and the noise level can be approximated as equivalent to the non-degenerated case. In the case of the PNP the thermal noise of the degeneration resistors is slightly less than that of the PNP shot noise sources and serves to reduce the white noise levels. However, for the non-degenerated reference using PNPs,

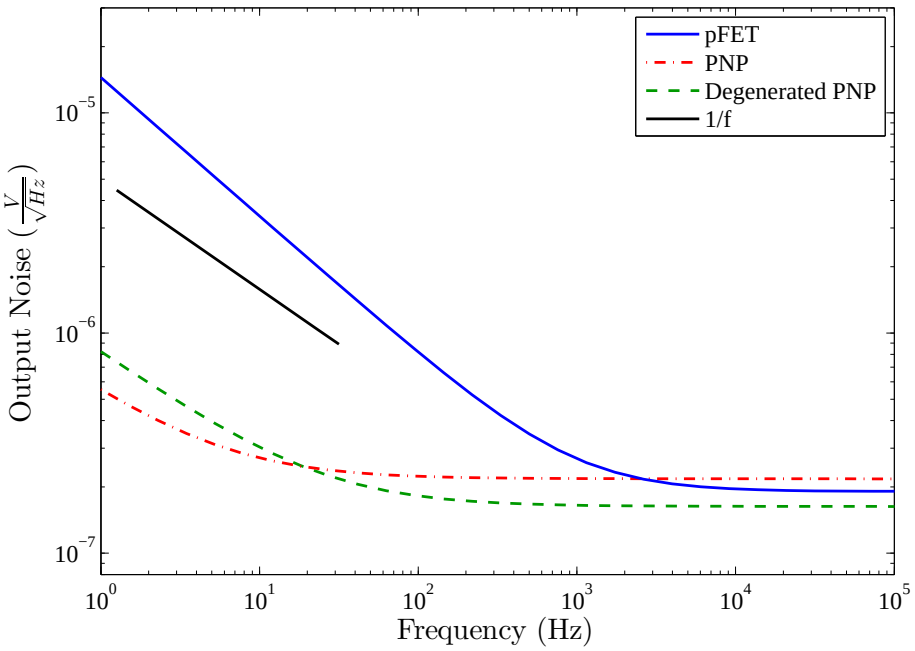

Figure 2.8: Simulated output noise for simple BGR circuit.

the simulated white noise level was 218 $nV/\sqrt{Hz}$ and the theoretical estimated white noise level was 200 $nV/\sqrt{Hz}$ at room temperature.

Fig. 2.8 shows the simulated noise performance of the three circuit variants. The significance of the pFET contribution to low frequency noise can be clearly seen in the order of magnitude difference between the pFET and PNP circuit noise. Additionally, the resistors degenerating the PNP devices reduce the white noise while contributing additional flicker noise.

2.2.3 Widlar BGR Design

As stated previously, the simple BGR implementation described in the previous section directly mirrors any noise from the PTAT current generator and amplifies it at the output. One solution to this problem is to select a topology such that the noise from the current reference is shunted into a low impedance path, and only the voltage generator contributes significantly to the noise. The circuit shown in Fig. 2.9 is a simplified band-gap reference based on Widlar's original design. The current reference used to bias the voltage generating cell was the I_{PTAT} reference previously described, and the additional cell and

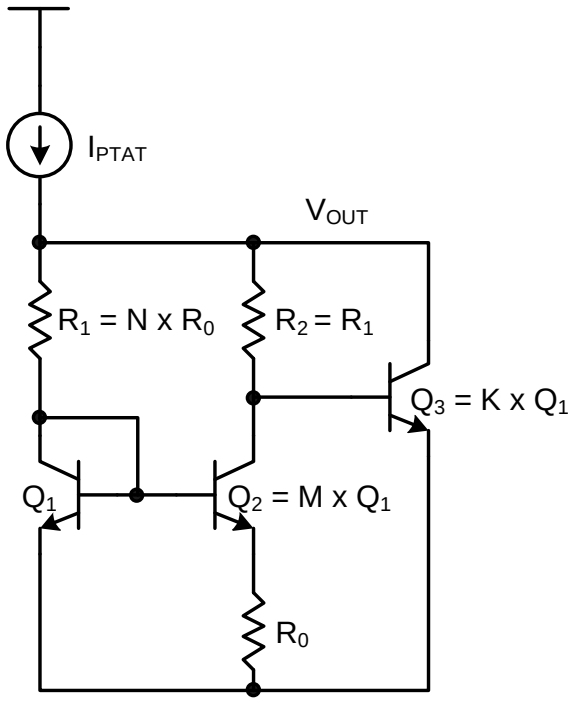

Figure 2.9: BGR topology based on Widlar design.

mismatched current mirror was sized identically to the mismatched current mirror in the current reference.

2.2.3.1 Noise Analysis

In order to calculate the theoretical noise performance of the second BGR topology, the same technique used in the previous section was employed, and the transimpedance gain from each node to the output voltage was first calculated. Additionally, in order to simplify the equations used in the derivation of each transimpedance gain two additional parameters will be introduced, R_F and G_{MF}, which are algebraically defined in Eqs. 2.17 & 2.18. Fig. 2.10 schematically shows the locations of each test current source as well as the equivalent circuit used in the derivation of the transimpedance gains of i_{t1} and i_{ref}.

$$G_{MF} = \frac{g_{m2}}{1 + \ln M}\left(\frac{\beta_3 R_2 - r_{\pi 3}}{R_2 + r_{\pi 3}}\right) \tag{2.17}$$

$$R_F = \frac{R_2 + r_{\pi 3}}{1 + \beta_3} \tag{2.18}$$

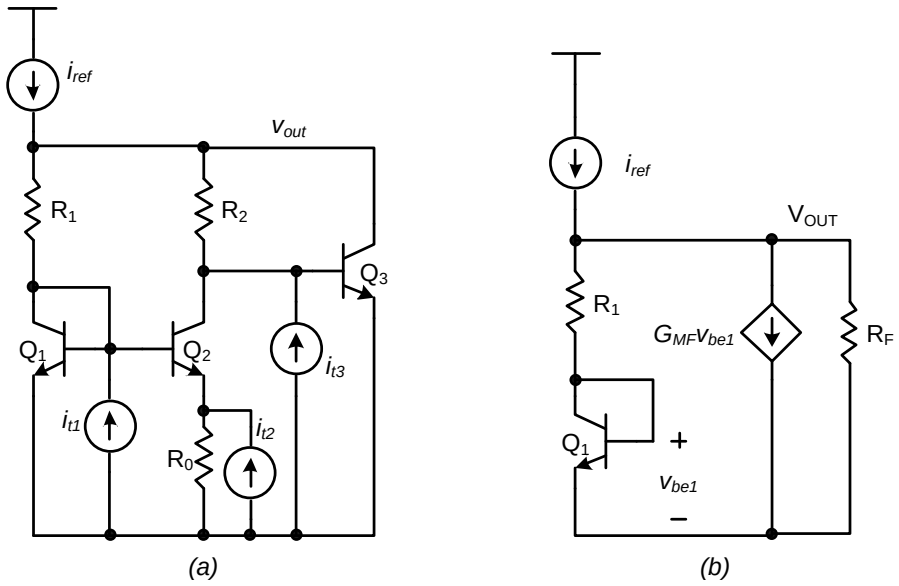

Figure 2.10: Test current sources and equivalent circuit used in noise derivation.

Using the equivalent circuit from Fig. 2.10(b), a single node equation can be solved to find the transimpedance gain of the reference current, defined as $A_{T.REF}$, which results in Eq. 2.19. Note that $g_{m2} = g_{m1}$ and has been substituted in the following equation.

$$A_{T.REF} = \frac{v_o}{i_{ref}} = \left\{ \frac{1}{R_F} + \frac{g_{m1}}{1 + g_{m1}R_1} \left[1 - \frac{1}{1 + \ln M} \left(\frac{R_2\beta_3 - r_{\pi 3}}{R_2 + r_{\pi 3}} \right) \right] \right\}^{-1} \tag{2.19}$$

Using the same equivalent circuit, the transimpedance gain of test current source i_{t1} to the output (A_{T1}) can also be derived, resulting in Eq. 2.20 (note that α is defined as $\frac{\beta}{\beta+1}$).

$$A_{T1} = \frac{v_o}{i_{t1}} = \frac{\alpha}{g_{m1}} \left[1 - \frac{(1 + g_{m1})(1 - R_F G_{MF})}{1 + g_{m1}(R_F + R_1) - G_{MF}R_F} \right] \tag{2.20}$$

Reverting back to the circuit of Fig. 2.10(a), a node equation can be used to solve for the transimpedance gain of i_{t3}, shown in Eq. 2.21.

$$A_{T3} = \frac{v_o}{i_{t3}} = \frac{R_2(1 + g_{m1}R_1)}{\frac{g_{m1}R_2}{1+\ln M} - 1 - g_{m1}R_1 + \frac{r_{\pi 3}+R_2}{r_{\pi 3}-\beta_3 R_2}[1 + g_{m1}(R_1 + R_2)]} \tag{2.21}$$

The gain of i_{t2} was derived by solving for the voltage gain of a voltage source in series with R_0 and then using a Norton equivalency to transform the voltage source into the current source i_{t2}. An open-closed loop feedback technique was used to solve for the voltage gain.

Note that it has been assumed that $r_{\pi 2} \gg 1/g_{m1}$ and the base degeneration of transistor Q_2 is negligible. It is also assumed that $g_{m1} = g_{m2}$ and can be substituted. The open loop gain is found by breaking the the connection between the bases of Q_1 and Q_2, resulting in the gain expression in Eq. 2.22

$$A_{V2.OL} = \left.\frac{v_o}{v_{t2}}\right|_{OL} = \left.\frac{v_o}{i_{t2}R_0}\right|_{OL} = -\frac{1}{1+\ln M}\frac{(1+g_{m1}R_1)(\beta_3 R_2 - r_{\pi 3})}{r_{\pi 3}+\beta_3 R_1 + r_{\pi 1} + R_2} \tag{2.22}$$

The feedback gain from the output to the base of Q_2 is a simple voltage divider, as shown in Eq. 2.23.

$$\beta_{fb2} = \left.\frac{v_{b.Q2}}{v_o}\right|_{OL} = \frac{1}{1+g_{m1}R_1} \tag{2.23}$$

Finally, the closed loop voltage gain can be calculated and converted to transimpedance gain as in Eq. 2.24.

$$\begin{aligned} A_{T2} = \frac{v_o}{i_{t2}} &= \frac{v_o}{i_{t2}R_0} \times R_0 = A_{V2.CL} \times R_0 = \frac{A_{V2.OL}R_0}{1+A_{V2.OL}\beta_{fb2}} = \frac{A_{V2.OL}R_0}{1-|A_{V2.OL}\beta_{fb2}|} \\ &= -R_0 \times \frac{(1+g_{m1}R_1)(\beta_3 R_2 - r_{\pi 3})}{(1+\ln M)(r_{\pi 3}+r_{\pi 1}+\beta_3 R_1 + R_2) + r_{\pi 3} - \beta R_2} \end{aligned} \tag{2.24}$$

Using the derived transimpedance gain expressions, whose validity was verified via comparison to simulation results, it is possible to then account for each noise source in the circuit and calculate an expected noise level at the output. The overall expression for the mean square noise voltage at the output is given in Eq.2.25, where the device numbers are defined in Fig. 2.9 and $\overline{i_{n.iptat}{}^2}$ is described in Eq. 2.15.

$$\begin{aligned} \overline{v_{n.out}{}^2} = \quad & \left(\overline{i_{shc1}{}^2} + \overline{i_{fb1}{}^2}\right) A_{T1}{}^2 + \left(\overline{i_{tr1}{}^2} + \overline{i_{fr1}{}^2}\right)(A_{T.REF} - A_{T1})^2 + \\ & \left(\overline{i_{tr2}{}^2} + \overline{i_{fr2}{}^2}\right)(A_{T.REF} - A_{T3})^2 + \left(\overline{i_{tr0}{}^2} + \overline{i_{fr0}{}^2}\right) A_{T2}{}^2 + \\ & \overline{i_{shc2}{}^2}(A_{T3} - A_{T2})^2 + \overline{i_{fb2}{}^2}(A_{T1} - A_{T2})^2 + \\ & \left(\overline{i_{n.iptat}{}^2} + \overline{i_{shc3}{}^2} + \overline{i_{fb3}{}^2}\right) A_{T.REF}{}^2 \end{aligned} \tag{2.25}$$

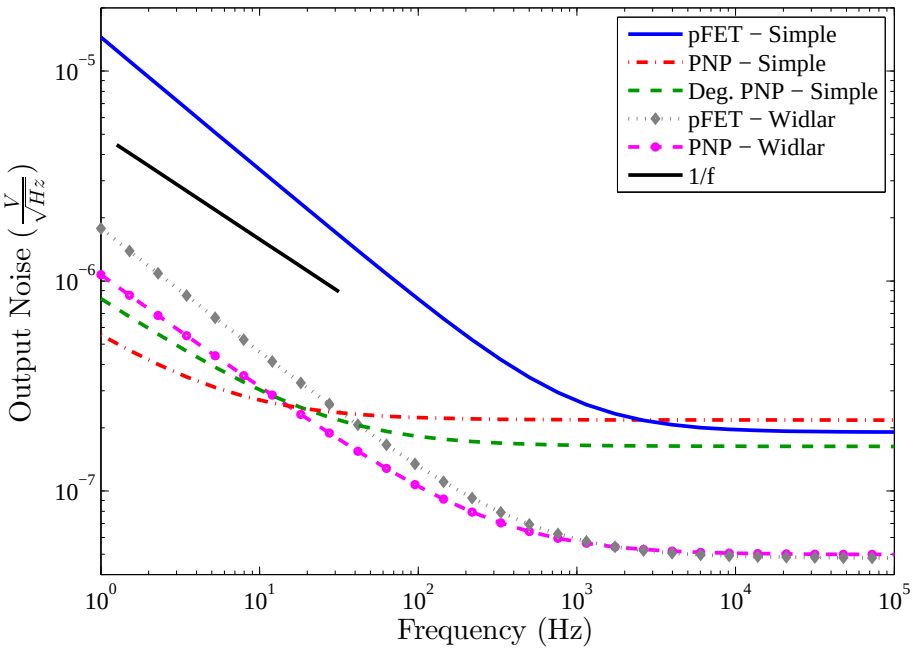

Figure 2.11: Simulated output noise curves for all fabricated BGR variants.

Using the previously described equations and substituting physical quantities and design values, the expected noise of the circuit using the pFET and PNP version of the PTAT current source was 47.5 $nV/\sqrt{Hz}$ and 48.4 $nV/\sqrt{Hz}$, respectively, while the simulated values were 48.0 $nV/\sqrt{Hz}$ and 49.8 $nV/\sqrt{Hz}$, respectively, showing excellent agreement.

Fig. 2.11 illustrates the advantage of the second topology, the two variants of which achieve nearly identical low frequency noise levels regardless of which devices are used in the PTAT current generator. The transimpedance gain of the current reference is much less than that of the other noise sources in the circuit, and the overall noise is limited by the NPNs and resistors in the voltage generation cell, rather than the p-type transistors in the current mirror. The Widlar type circuits also use significantly smaller devices than the simple BGR circuits, with comparable $1/f$ noise (recall that larger devices have less $1/f$ noise than a smaller device at the same current).

2.2.4 Expected Cryogenic Performance

As stated previously, commercial devices are not modeled at cryogenic temperatures, and theoretical derivations were necessary to project the circuit performance at their operating

Table 2.1: Simulated vs. Calculated BGR White Noise Output Voltage Levels (Units in $nV/\sqrt{Hz}$)

	PFET (Simple)		PNP (Simple)		PFET (Widlar)		PNP (Widlar)	
Temp.	Sim.	Calc.	Sim.	Calc.	Sim.	Calc.	Sim.	Calc.
25°C	191	185	218	200	48.0	47.5	49.8	48.4
0°C	186	180	212	196	46.6	46.3	48.3	47.1
-25°C	180	175	206	188	45.2	44.9	46.7	45.7
-55°C	173	168	198	181	43.4	43.1	44.6	43.9
-183°C		118		126		29.4		29.5

temperature of 90K. The white noise levels are determined by shot and thermal noise, which are well defined and do not vary with process parameters, and Tab. 2.1 shows the theoretically calculated output noise values alongside the simulated noise levels. At the 90K (183°C) data point, simulation data is not available and only the theoretically predicted value is shown.

Calculating the theoretical low frequency noise levels was not feasible because the low frequency noise parameters and coefficients are statistical in nature and may vary significantly between otherwise identical circuits and devices. However, the relative differences in circuit noise levels and the previously detailed circuit analyses do give some insight into the origins of the $1/f$ noise spectrum of the BGRs. Clearly, the pFETs contribute the overwhelming majority of $1/f$ noise to the circuit variants containing such devices. Additionally, the excess noise contributed by the resistors is significant in the circuits using only bipolar devices.

2.3 Circuit Measurements

The five BGR circuit variants were fabricated in IBM's 7WL BiCMOS process, which is a 0.18 μm process offering SiGe HBTs with a cutoff frequency of up to 60GHz, vertical silicon PNPs, and an assortment of CMOS devices. The pFETs used in previously described designs were rated at 3.3V with a minimum gate length of 400nm. Once the circuits had been fabricated and diced, they were wirebonded into dual inline pin (DIP) packages compatible with the cryogenic dewar systems used for low temperature measurements.

For measurements requiring controlled temperatures, a helium based closed-cycle refrigeration system was primarily used. The packaged circuits were placed in a vacuum chamber with thermal contact to the refrigeration system. Additionally, a LakeShore 331 Temperature Controller was used to monitor the temperature and apply heating as needed to maintain the proper temperature setpoint. Due to the sensitive nature of noise measurements, it was difficult to determine the exact effects of the refrigeration system on the measured noise of the circuit, and a second set of noise measurements were taken using an open cycle liquid nitrogen cooled dewar system.

2.3.1 DC Characteristics

The DC measurements of the BGR circuits were performed using an Agilent 4155C Semiconductor Parameter Analyzer to both supply the rail voltage and measure the output voltage and power consumption.

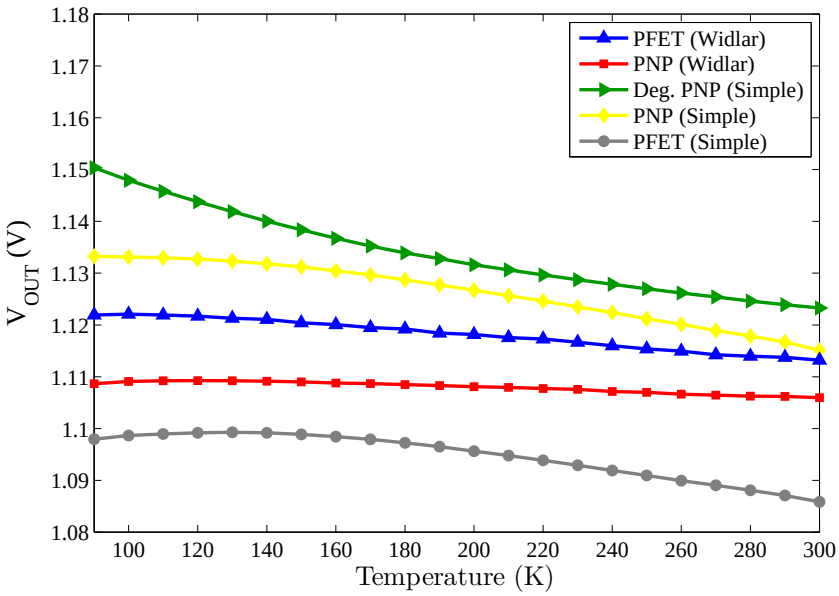

Figure 2.12: Measured output voltage vs. temperature characteristics for five BGR circuits ($V_{CC} = 2.1V$).

The targeted output voltage of the BGRs at 90K was 1.12V, which, as discussed previously, was found in practice to be the zero temperature coefficient value. Fig. 2.12 shows the measured temperature characteristics, and for most circuits, the flat region of the curve

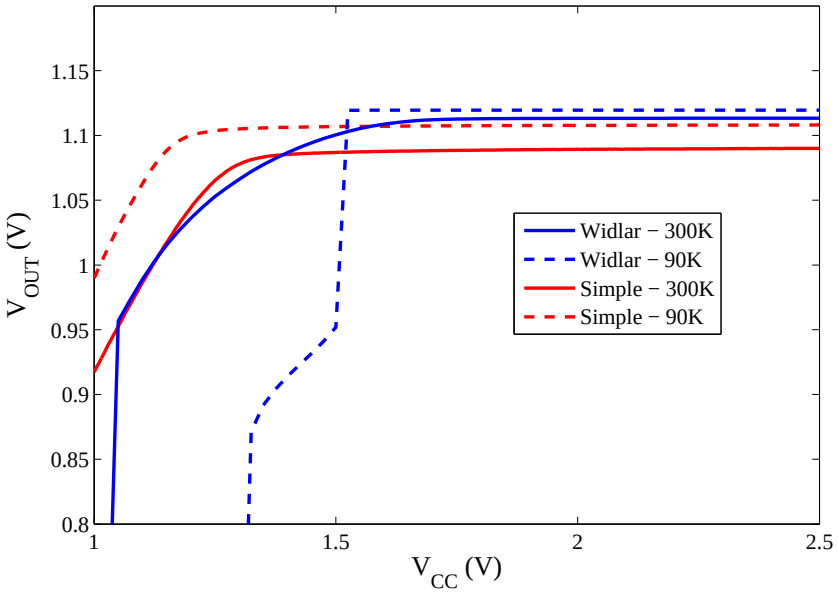

Figure 2.13: Measured output voltage vs. supply voltage for simple and Widlar-type circuits.

is indeed close to the desired 90K operating point. For the circuits shown, the worst temperature coefficient (TC) was 117 ppm/$^{\circ}C$ and the best TC was 13 ppm/$^{\circ}C$ (both values were calculated using the box method), which is typical for first order, untrimmed band-gap references [24].

Despite an increase in transistor turn-on voltages at low temperatures, all circuits operated correctly at 2.1V, and Fig. 2.13 shows the output voltage as a function of supply voltage for two representative circuits (the main variation in response was caused by structural changes, and the PNP vs. pFET variants did not differ appreciably in this regard).

2.3.2 Noise Characteristics

Noise measurements were made using an HP 35670A Dynamic Signal Analyzer (DSA), which was capable of measuring spectral content from below 1 Hz to roughly 50 kHz, fed by a low noise amplifier with an input referred noise at least an order of magnitude lower than the noise of the BGR circuits in question. The addition of the amplifier serves to reduce the noise levels of spurious signals relative to signal to be measured.

Room temperature measurements were performed on a simple breadboard to minimize

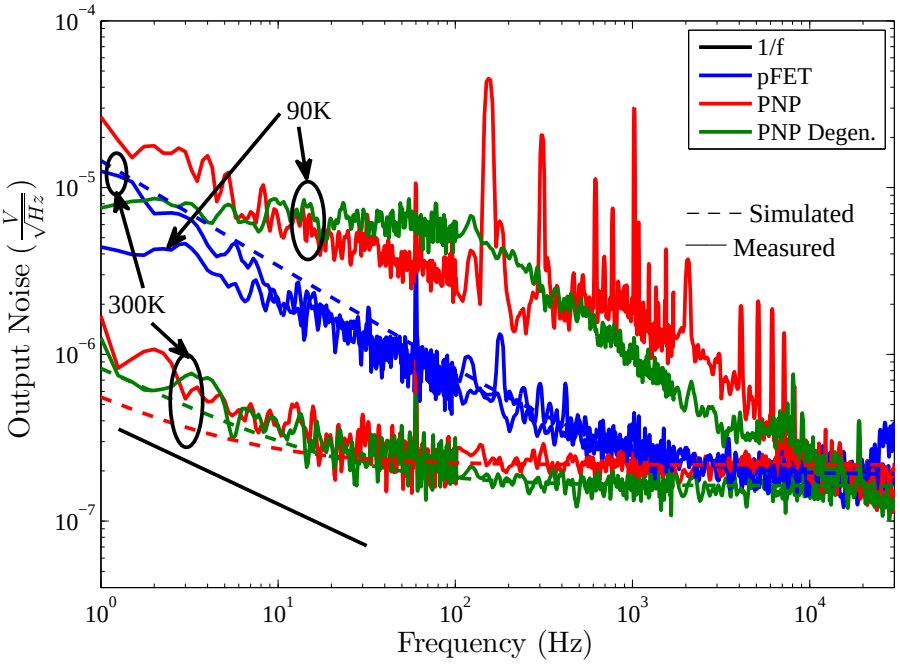

Figure 2.14: Comparison of simulated and measured output noise for simple BGR variants.

ground pollution, and the DSA was powered through a filtered 60Hz, 120VAC power supply. For all noise measurements, the circuits were powered using low noise 2.1V lead-acid batteries to avoid supply injected noise.

Cryogenic measurements were initially performed using a closed-cycle helium refrigeration system. However, due to the sensitive nature of noise measurements, it was difficult to determine the exact effects of the refrigeration system on the measured noise of the circuit, and a second set of measurements were taken using an open cycle liquid nitrogen cooled dewar system. Both cryogenic measurement systems, however, showed similar added noise levels.

Fig. 2.14 shows the overlaid measured and simulated output noise of the simple BGR variants at room temperature as well as the measured output noise at 90K. The room temperature noise of all three circuits matches simulation quite well at high frequencies, and only the PNP mirror variant shows a slight deviation at low frequency. At cryogenic temperatures, however, the low frequency noise increases dramatically for the circuit variants incorporating PNPs and in one case shows a spectrum consistent with G/R or RTS noise.

Fig. 2.15 shows the overlaid measured and simulated output noise of the Widlar-type

BGR circuits. A trend similar to that observed in Fig. 2.14 is present, and the circuit employing a pFET mirror closely matches the simulated value, while the variant designed with PNP mirrors shows slightly higher than expected noise levels. Additionally, as in the first case, both circuits show substantially increased noise at cryogenic temperatures.

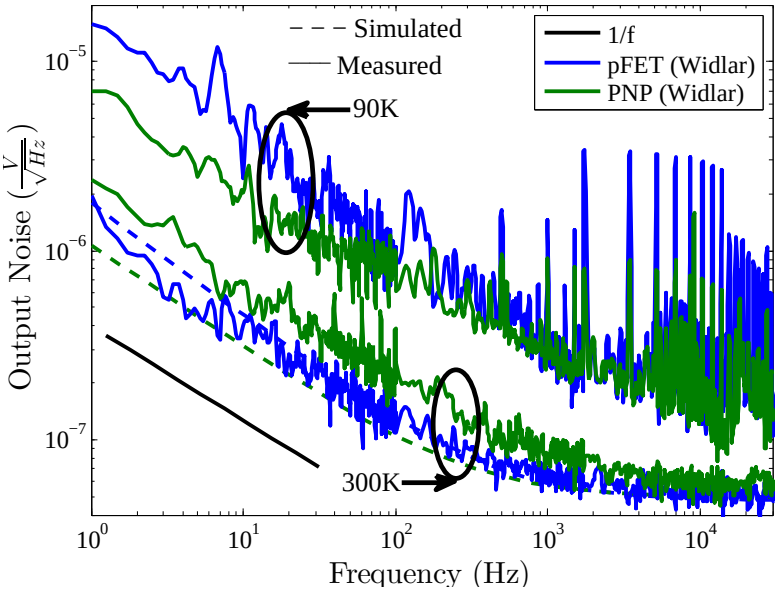

Figure 2.15: Comparison of simulated and measured output noise for Widlar BGR variants.

2.4 Results & Analysis

Both cooling systems used to control the temperature of the circuits under test presented some difficulties in accurately characterizing the circuit noise. The measured results in Figs. 2.14 & 2.15 show significant added noise at frequencies above roughly 100 Hz. It was found that the source of the added noise was the ground connection of the band-gap circuit, which, in both measurement systems was connected to the dewar. The noise was likely coupled in from ground loops created by the physical chamber and accessories required to cool the chamber (cryogen dewars, vacuum pumps, compressor, etc.). Unfortunately, due to the construction of the dewars, it was not possible to isolate the ground terminals and disconnect the sources of the noise. This substantially reduces the accuracy of any high

frequency (greater than roughly 100 Hz) noise measurements, but the low-frequency noise spectra remained clean of extraneous noise. Additionally, because the white noise sources are not dependent on temperature, the low temperature noise levels listed in Tab. 2.1 should remain valid, and the overall noise performance can be extrapolated from the low frequency data and the calculated values.

While previous studies have shown that the low-frequency noise in polysilicon bipolar transistors show some increase at low temperatures [38] [37], the BGR circuits use a PTAT current reference, and the overall DC current in each device in the circuit decreases with increasing temperature. Additionally, any temperature induced variation in resistances will also be translated into a current variation. Given a three-fold decrease in temperature and negative temperature coefficient resistors, the bias current was expected to decrease by a factor of roughly four, which was consistent with measurement. The decrease in bias current and an increase consistent with the results of [38] should have resulted in a minimal change reduction in $1/f$ noise levels, which vary proportionally to ${I_{DC}}^2$. However, as shown in Figs. 2.14 & 2.15, there was nearly an order of magnitude increase in the noise of some circuits.

As discussed previously, the low frequency noise of the simple BGR (a PTAT current source driving a series diode-resistor load) employing pFETs is dominated by the noise of the CMOS mirror devices. The low temperature noise of said circuits did not show the same increase in magnitude that PNP circuits demonstrated, indicated that the intrinsic noise coefficient of the pFETs may have increased slightly to counter the reduction in DC current. However, the circuits employing PNP transistors had higher absolute noise than their CMOS counterparts, indicating that the PNP transistors, not the resistors and NPN devices, are the cause of the drastic increase in noise. Additionally, the degenerated PNP circuit shows a large G/R noise component that did not appear at room temperatures.

In the Widlar BGR variant, the noise of the mirror was shown to be attenuated, and the NPN transistors and resistors in the voltage generation cell were significant contributors to the output noise. However, at cryogenic temperatures, the relative performance of the PNP and pFET mirror circuits seems to counter the results of the simple variants. Additional

circuits fabricated on the same wafer were measured, but the results remained consistent across circuit measurements. However, it should be noted that low-frequency noise coefficients, and G/R or RTS noise levels in particular are highly device dependent and may vary substantially depending on fabrication. Additionally, the simple BGR circuits and the Widlar variants were fabricated during different process runs, which could possibly impact device performance.

2.5 Conclusions

The measured results indicated a substantial increase in the flicker noise coefficients of both the pFET and PNP transistors at cryogenic temperatures. It is also possible that the SiGe NPN transistors and/or resistors may also have shown an increase in low frequency noise, although additional device level measurements are needed for verification. These results show that while thermal noise may decrease and device performance may increase at low temperatures, increases in low-frequency noise may offset said performance gains, especially in a circuit context where input referred noise is not a relevant metric (e.g. a BGR). The presented results clearly demonstrate that more work is need to fully understand the behavior of device low-frequency noise at cryogenic temperatures. Due to the statistical nature of device fabrication and hence low-frequency noise characteristics, a large sampling of devices may be necessary to fully characterize the noise capabilities of a process at cryogenic temperatures.

CHAPTER III

EVALUATION OF A 0.18 MICRON SIGE BICMOS TECHNOLOGY PLATFORM FOR USE IN AN UNSHIELDED EUROPA ENVIRONMENT

This chapter details the testing of a previous uncharacterized radiation hardness of a SiGe BiCMOS platform against dose levels comparable to those encountered during a deep space exploration mission, specifically Europa. Both SiGe HBTs and complementary CMOS devices were subjected to both X-ray and proton beams, and the total dose effects are compared to those of previously published results.

3.1 Introduction

As previously discussed, Silicon-Germanium (SiGe) BiCMOS technology has seen growing attention as a potential platform for space-capable circuits and electronics [7]. The low temperature characteristics, intrinsic tolerance to total ionizing dose (TID) radiation, and compatibility with established CMOS technology nodes of SiGe HBTs make them ideal for radiation hard system-on-a-chip applications. Past studies on the TID tolerance of SiGe BiCMOS processes have shown multiple generations of SiGe HBTs to be radiation hard to multi-Mrad(SiO_2) levels [8][9][27][6]. Additional studies have focused on the CMOS devices fabricated together on-die with these SiGe HBTs (to form the BiCMOS platform), but only evaluating the TID response up to a few hundreds of krad(SiO_2) [25], which is sufficient for most orbital missions. However, some emerging deep space exploration missions, specifically those involving the outer planets and their moons (e.g., Europa), will require multi-Mrad hardness for any components operating outside of the shielded electronics vault [5]. The present study evaluated the TID tolerance of Jazz Semiconductors $0.18\mu m$ SiGe BiCMOS (SBC18-HXL, with 150 GHz peak fT) process and its potential suitability for multi-Mrad operation needed to support future Europa missions. This technology is a triple-well variant of the standard substrate process presented in [6], which demonstrated a preliminary

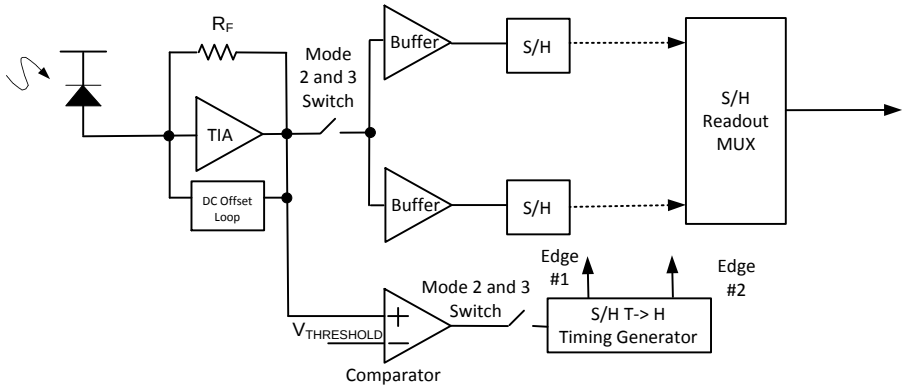

Figure 3.1: Block diagram of conceptual FPA design.

evaluation of the SiGe HBT proton tolerance.

3.1.1 Motivation

This study was performed as part of a greater effort to evaluate the feasibility of developing an unshielded focal plane array (FPA) for use in proposed Europa exploration missions [5][1][26]. These FPAs can be used for infrared detection without the need for a shielded warm-box, and require a full suite of p-type and n-type MOSFETs in addition to SiGe HBTs (a simplified conceptual design is shown in Fig. 3.1).

Due to the die area and pitch/density requirements of pixel arrays, the use of annular MOSFETs for TID damage mitigation is unlikely to be feasible due to increased area consumption.

3.1.2 Experimental Goals

This study evaluated the performance degradation of the unhardened CMOS devices implemented in the Jazz SBC-18 HXL process up to the 6 Mrad(SiO_2) dose that must be survived over the lifetime of a Europa exploration mission. The SiGe HBTs, though expected to be radiation hard based on prior published work, were likewise tested at the same dose.

3.2 Experimental Parameters

Minimum length (180 nm) CMOS devices (both nFET and pFET) of varying widths and SiGe HBTs of various emitter geometries were irradiated up to 6 Mrad(SiO_2) using a 10-keV X-ray source. The devices were measured at intermediate dose points immediately following irradiation. In order to corroborate the X-ray results, a second set of nFETs and SiGe HBTs were also irradiated up to an equivalent 3 Mrad(SiO_2) dose using the 63.3 MeV proton source at UC Davis, which has been described in [4], and the nFETs were measured at intermediate dose points immediately following irradiation. For both experiments, all FETs were biased with the maximum rated gate voltage applied and all other terminals grounded (i.e., worst case conditions), and all SiGe HBTs were irradiated with all terminals grounded (also worst case).

3.3 Results and Analysis

Pre-radiation measurements are presented and compared to post-radiation device characteristics. Results are also compared to previously published results, and explanations are offered for the differences.

3.3.1 HBT TID Effects

Fig. 3.2 shows the response of the irradiated SiGe HBT. The primary degradation mechanism in the forward characteristics of this device is the generation of traps at the EB spacer oxide/EB space charge region interface, as expected. The traps in the EB spacer oxide generated by the ionizing radiation result in excess recombination current with a characteristic 2kT slope (shown in Fig. 3.3 for both the X-ray and proton exposures. As expected, the magnitude of the excess leakage current is positively correlated with increasing emitter geometries.

While the absolute level of leakage increases with increasing geometry, the data in Figs. 3.3 and 3.4 indicate that SiGe HBTs with wider emitter stripes (i.e. a lower perimeter-to-area ratio) are more resistant to current gain degradation than narrow stripe devices, a result that is consistent with a past study on custom geometry SiGe devices [2]. In

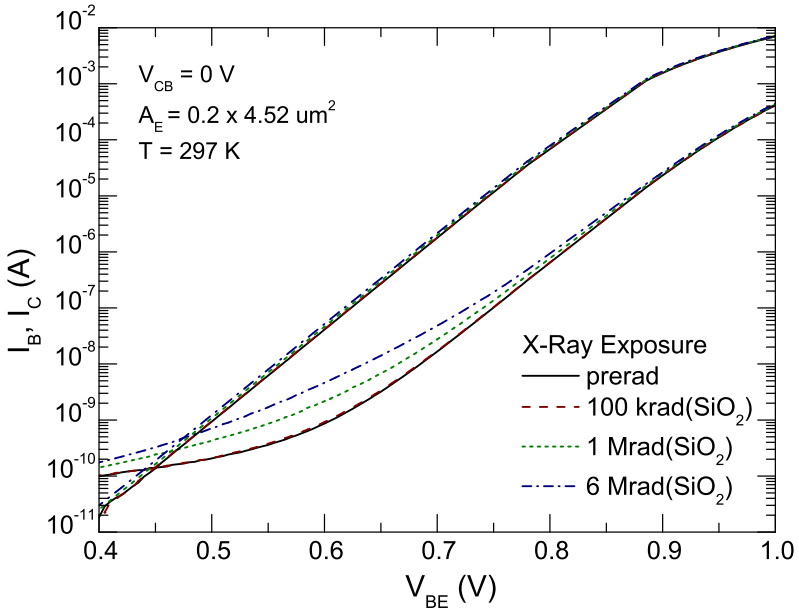

Figure 3.2: Forward Gummel curve of Jazz HBT showing radiation induced degradation.

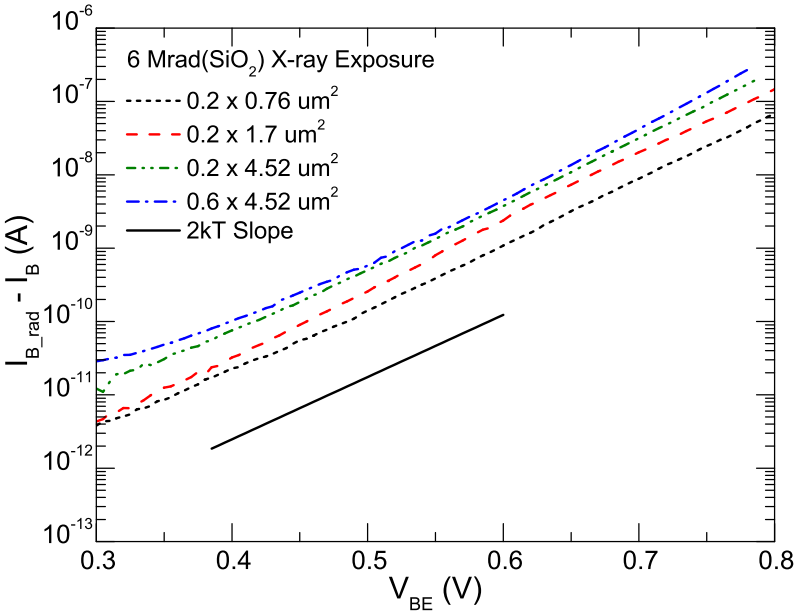

Figure 3.3: Excess base current in SiGe HBTs of various geometries after 6Mrad(SiO_2) X-ray exposure.

most commercial SiGe technologies, the emitter stripe width is a fixed parameter and this effect is not observable, but the Jazz SBC-18 HXL platform allows for use of three distinct emitter widths. Increasing the emitter width improves the radiation hardness at the cost of increased parasitics, but this potential tradeoff allows greater flexibility in designing radiation tolerant circuits and further increases the utility of this SiGe process for use in unshielded, Mrad-hard electronics.

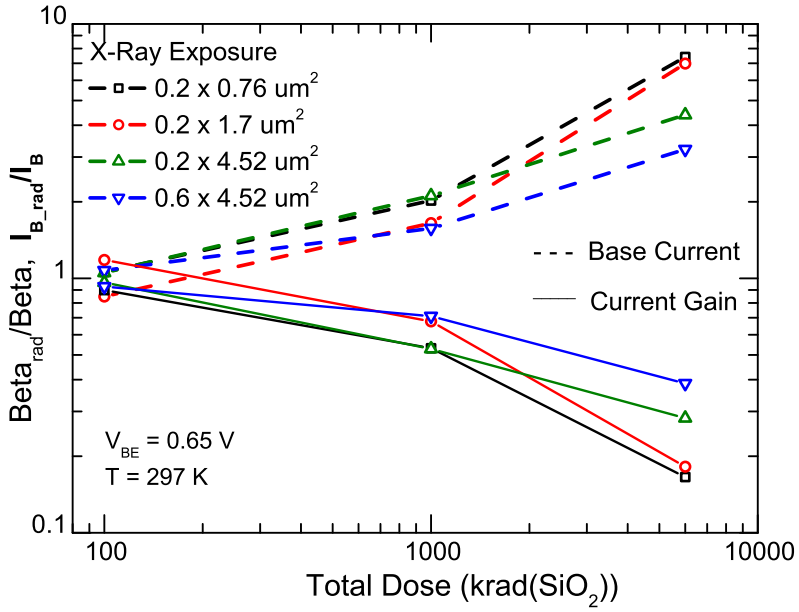

Figure 3.4: Normalized base current and current gain degradation in SiGe HBTs of various geometries after 6Mrad(SiO_2) X-ray exposure.

3.3.2 CMOS TID Effects

The radiation responses of the CMOS devices show a marked improvement over the previously published response of a similar SiGe BiCMOS technology at an identical lithography node, shown in Fig. 3.5.

Fig. 3.6 shows the total dose response of the drain current of a wide (10 μm/0.18 μm) nFET as the gate-source voltage is swept. The X-ray and proton responses of all FETs were similar, with the proton exposure resulting in slightly greater degradation. The lack of threshold voltage shift, even at very high dose levels, indicates that there is little to no charge trapped in the gate oxide. The observed degradation is caused primarily by charge

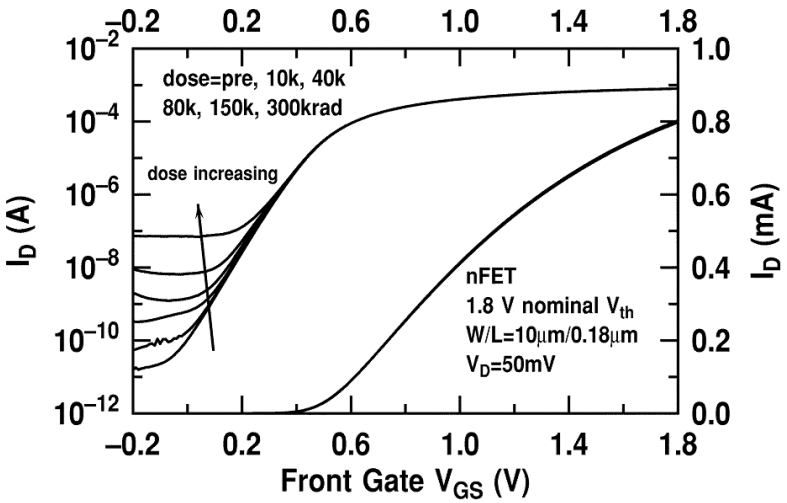

Figure 3.5: Previously published TID response of nFET implemented in a SiGe BiCMOS platform (After [25])

in the shallow trench isolation (STI) oxide and its interface with the channel region.

The device shows significantly different degradation characteristics than those of the identically sized nFET shown in Fig. 3.5, with the leakage of the present technologys nFET showing a much stronger V_{GS} dependence. The previously published device response also shows a more classical off-state leakage characteristic independent of V_{GS}, consistent with charge trapping deep along the STI edge, which creates a parasitic inversion channel far removed from the upper STI corner, inducing a shunt leakage path between source and drain. Previous studies have also shown that STI corner leakage causes a sub-threshold hump in the I_D-V_{GS} characteristics, while deep STI leakage results in a flat, constant leakage current [29][33]. In [33], a strong dependence of the leakage characteristics on the spatial distribution of the charge in the STI and at the STI/bulk Si interface was reported, offering some explanation of the comparative results.

The factors responsible for the different responses of the nFETs from two different SiGe BiCMOS technologies with comparable lithography and performance may also include both doping and structural differences. Higher doping concentrations reduce the susceptibility of the well to STI edge inversion, and the physical structure of the STI dictates the electric field contours and gate-STI interactions. One known difference between the two BiCMOS platforms is the shape of the STI oxide, which, in the present BiCMOS technology, exhibits

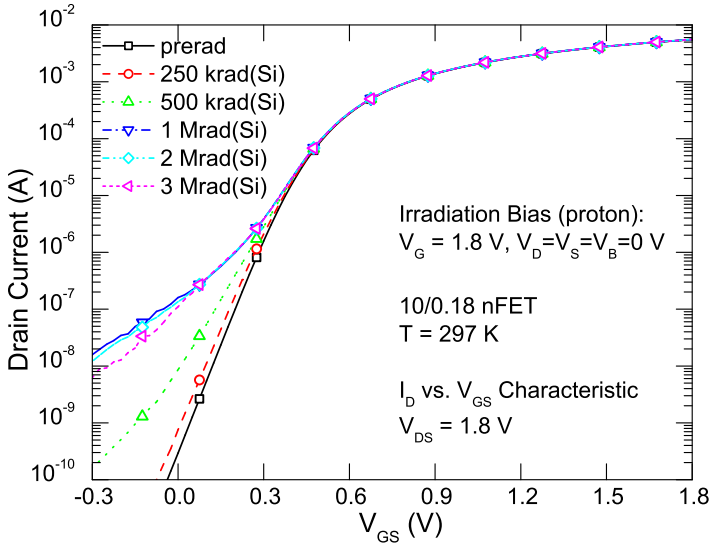

Figure 3.6: TID response of the I_D-V_{GS} curve of a wide nFET

both a slightly recessed top surface (the gate dips down as it crosses the STI channel edge) and a retrograded, or inward-sloped, shallow trench edge, while the STI trench structure found in [25] is nearly vertical.

While the TID responses of the nFETs in question differ from those found in [25], their responses are consistent with other bulk CMOS platforms found in the literature (presumably with STI shapes similar to those found in the present technology). Fig. 3.7 shows the leakage characteristics for a narrow nFET, and Fig. 3.8 shows the threshold response (extracted by extrapolating to zero from the linear region of the I_D-V_{GS} curve) of all irradiated CMOS devices. The STI leakage effects cause an apparent threshold voltage shift in the small devices, a result of radiation-induced narrow channel effects, as described in [11], since the edge structure and hence magnitude of the leakage current is roughly the same regardless of transistor width.

A rebound effect is also observed in the nFETs at high dose levels as charge also builds up at the oxide/Si interfaces. The radiation-induced interface charges are negative for a p-substrate (nFET) and positive for an n-type substrate or well (pFET) and form at a different rate than bulk STI oxide charges, which are responsible for the degradation at low values of total dose. In the pFETs, the positive interface charge reinforces the effect of the positive bulk STI charge, resulting in a slight increase in threshold voltage, the only observed

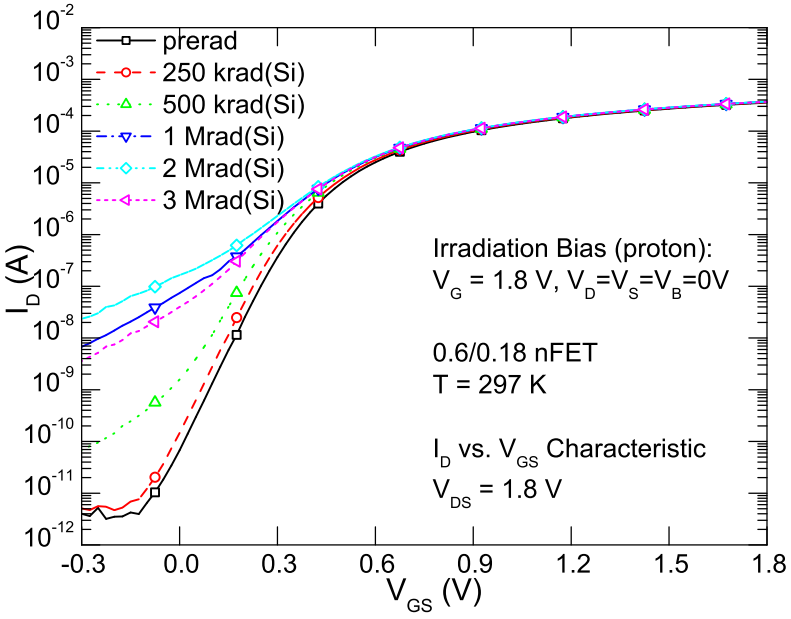

Figure 3.7: TID response of narrow nFET's I_D-V_{GS} curve at varying dose points

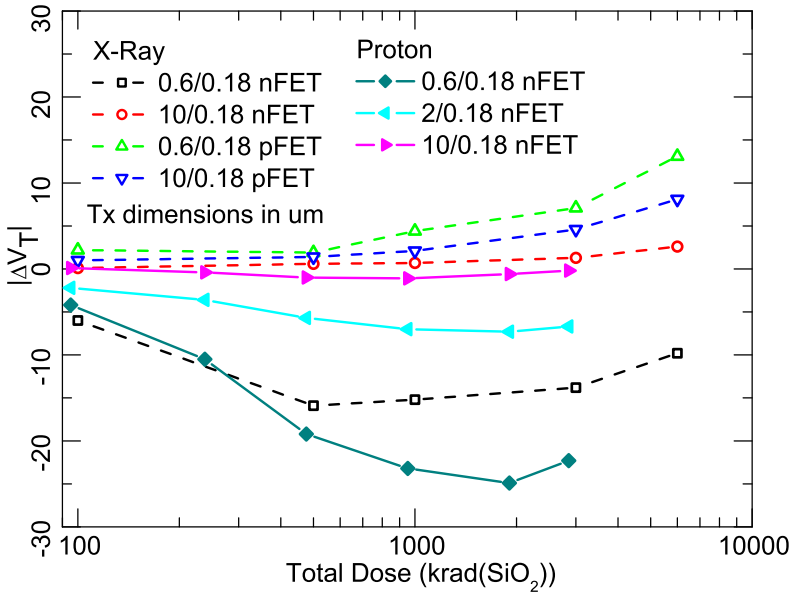

Figure 3.8: TID induced threshold voltage shifts

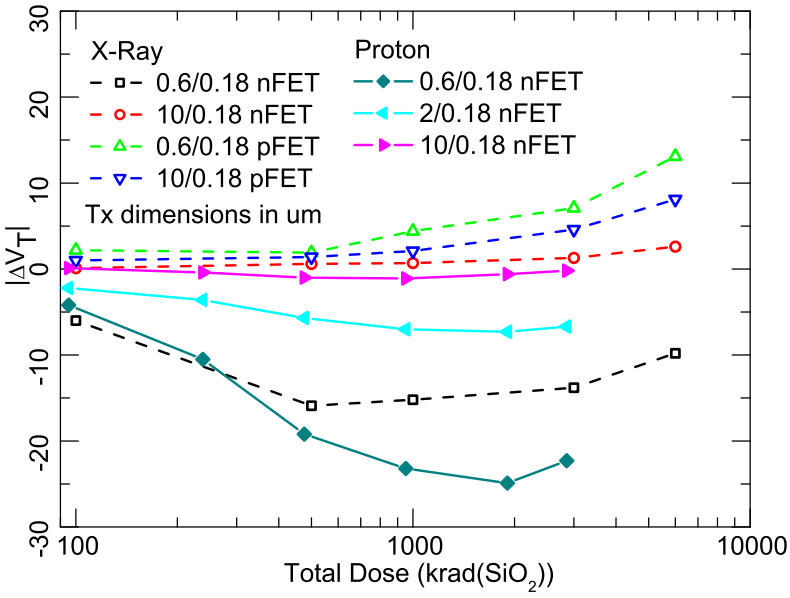

Figure 3.9: Radiation induced off-state leakage current

degradation seen in the pFETs at high total dose. In the nFETs, however, the interface charges are negative and counteract the positive bulk oxide charges at high total dose values [12], effectively improving the total dose tolerance of the nFETs, which is beneficial for operation of the nFET at the very high dose levels seen in a Europa environment. Other circuit relevant FET parameters, such as transconductance, did not show any appreciable degradation or shift above threshold, and the output characteristics of a wide nFET and pFET (Fig. 3.10) show very little degradation up to 6 Mrad(SiO_2), also a favorable result.

3.4 Summary

The total ionizing dose response of Jazz Semiconductors SBC18-HXL SiGe BiCMOS platform has be evaluated, and it has been demonstrated that this technology is capable of operation up to the extreme dose levels needed for operation in an unshielded Europa environment.

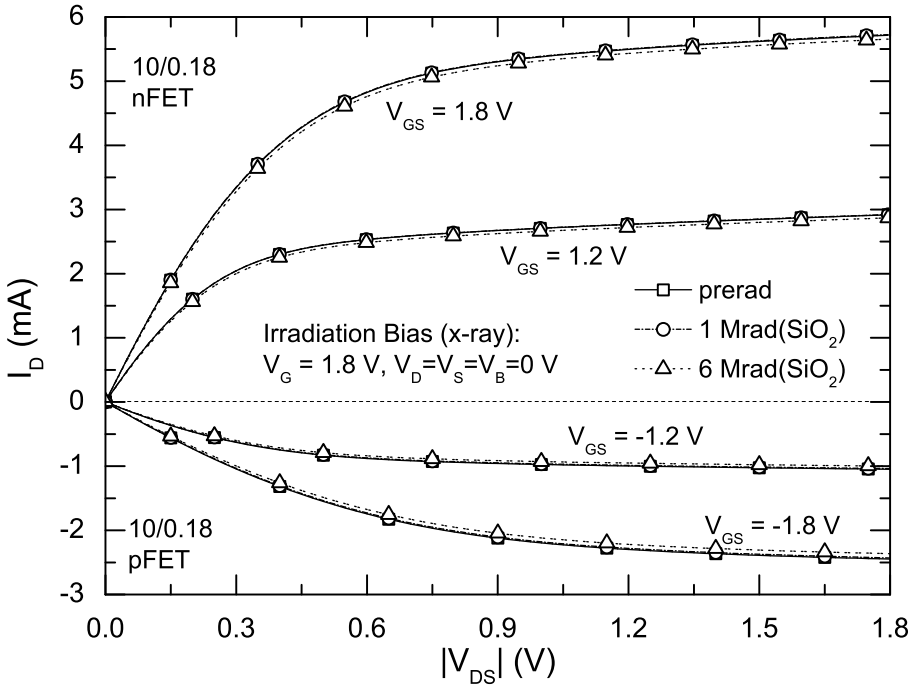

Figure 3.10: TID response of CMOS output characteristics

CHAPTER IV

CONCLUSIONS

The previous two chapters documented two studies highlighting the utility of SiGe BiCMOS technology for realizing extreme environment capable sensing circuitry. While both studies facilitated advances in understanding, they also raised questions that must be addressed in future work. Both of these will be summarized and addressed in the following sections.

4.1 Contributions

As discussed in Chapter 2, band-gap reference circuits are an integral part of any on-chip voltage regulation system. Silicon germanium technology is an excellent candidate for realizing and implementing the low-noise cryogenic voltage regulator targeted by this study, but the lack of modeling and simulation capabilities at the desired operating temperatures limit the ability to robustly design circuits. This work proposed several topology variants of band-gap reference circuits for use in such a system and performed detailed theoretical analysis allowing a designer to extrapolate the noise performance of such a circuit at the desired operating temperature. The circuits were found to behave according to expectation at room temperatures, but diverged at cryogenic temperatures. This result indicates that operating circuitry at cryogenic temperatures may not ultimately reduce system noise, depending on the frequencies of interest. The results also called into question the correlation between room temperature and cryo temperature device noise characteristics, but the analysis contained in Chapter 2 laid the groundwork for future device measurements, which would help to provide a more robust understanding of overall circuit performance.

Chapter 3 detailed a study of total ionizing dose radiation effects on a previously uncharacterized SiGe BiCMOS process. Both CMOS and bipolar devices demonstrated hardness up to the dose levels required for a Europan exploration mission, the application targeted by the study. This work is the first step in implementing circuit level, and eventually system level designs using the technology in question. The results of this study as presented in

this work have been accepted for presentation in July 2012 at the Nuclear and Space Radiation Effects Conference (NSREC) and will be submitted to the Transactions on Nuclear Science (TNS) for peer review and eventual publication in December 2012. Segments of the data from this study have also been incorporated into two other conference presentations, namely "An 8-16 GHz SiGe Low Noise Amplifier with Self-Healing Capability for Mitigation of Radiation-Induced Performance Loss," also accepted for presentation at NSREC 2012 and subsequent submission to TNS, and "An Investigation of Total Ionizing Dose Damage on a Pulse Generator Intended for Space-Based Impulse Radio UWB Transceivers," which has been accepted for presentation at the 2012 European Radiation Effects on Components and Systems Conference (RADECS) [18].

4.2 Future Research

The study presented in Chapter 2 highlighted the need for further understanding of low-frequency noise phenomena at cryogenic temperatures. The performance of any circuit is ultimately dependent on device characteristics, and anomalous circuit behavior at cryogenic temperatures is likely rooted in device-based physics. Further research into both $1/f$ and G/R noise at cryogenic temperatures is critical to properly understand circuit performance and ensure robust operation. Additionally, the development of a cryogenic measurement system capable of sustaining an isolated electrical ground would greatly improve the ability to measure low-frequency noise, particularly in the kiloHertz regime.

The study presented in Chapter 3 likewise represents the first step in ultimately designing circuits capable of operating in the harsh Europa environment using Jazz Semiconductor's SBC18 technology. Europa's ambient temperature is similar to the operating temperature of the circuitry described in Chapter 2, and circuits and systems designed for such a mission will face the same obstacles encountered in the design and characterization of the low-noise band-gap references. And finally, although the long-term radiation effects of DC device characteristics showed very promising results, radiation effects on device level noise performance as well as radiation induced single event effects must also be accounted for in any designs.

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